ELECTRICAL INSTABILITY OF a-Si:H/SiN THIN FILM TRANSISTORS

A STUDY AT ROOM TEMPERATURE AND LOW VOLTAGE STRESS

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ELECTRICAL INSTABILITY OF A-Si:H/SiN THIN FILM TRANSISTORS

A STUDY AT ROOM TEMPERATURE AND LOW VOLTAGE STRESS

DISSERTATION

To obtain
the doctor's degree at the University of Twente,
on the authority of the rector magnificus,
Prof. Dr. F. A. van Vught,
on the account of the decision of the graduation committee,
to be publicly defended on
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By

Andreea Ruxandra Merticaru
born on 22nd of September 1972
in Bucharest, Romania

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This dissertation is approved by promoters:

Prof. Dr. F.G.Kuper

Prof. Dr. A.J.Mouthaan

Things should be made as simple as possible, but not any simpler. (Albert Einstein)

To my parents
For all their years of patience dedicated to grow up me and my brother, for carefulness to share their knowledge and life experience with us.

LIST OF PUBLICATIONS

related to this thesis

1. A.Merticaru, H.van Kranenburg, A.J.Mouthaan **"Induced bias stress degradation on the a-Si:H TFT"** (SAFE Workshop, nov. 1999)
2. A.Merticaru, A.J.Mouthaan **"Study of dynamics of charge trapping in a-Si:H/SiN TFTs"** (SAFE Workshop, nov. 2000)
3. A.Merticaru, A.J.Mouthaan, F.G.Kuper **"Study of dynamics of charge trapping in a-Si:H/SiN TFTs"** (SAFE Workshop, nov. 2001)
4. A.Merticaru, A.J.Mouthaan **"Dynamics of metastable defects in a-Si:H/SiN TFTs"** (Thin Solid Films 383 (1-2), 122-124, 2001)
5. A.Merticaru, A.J.Mouthaan, F.G.Kuper **"Progressive Degradation in a-Si:H/SiN Thin Film Transistors"** (Thin Solid Films 427 (1-2), 60-66, 2003)
6. A.Merticaru, A.J.Mouthaan, F.G.Kuper **"Modelling long-term degradation in a-Si:H/SiN TFTs"** (submitted to IEEE-TED journal)
7. A.Merticaru, A.J.Mouthaan, F.G.Kuper **"Determination of the defect creation and charge trapping contributions on the degradation of a-Si:H/SiN TFTs electrical characteristics"** (to be submitted to Non-Crystalline Solid State Journal)

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New York Times 1st July 1948:

"A device called a transistor, which has several applications in radio where a vacuum tube ordinarily is employed, was demonstrated for the first time yesterday at Bell Telephone Laboratories, 463 West Street, where it was invented."

Abstract

The thesis shows the results of four years of research into the electrical stability of a-Si:H/SiN TFTs. Various methods of investigation of a-Si:H/SiN TFTs have been carried out in this thesis towards understanding the causes of degradation that shortens the transistor lifetime and narrows the transistor application area. The research aims to cast light on the mechanism responsible for a-Si:H/SiN TFTs degradation during short and long period of voltage stress at room temperature.

CHAPTER 1

INTRODUCTION

The first application for a patent on a device based on the so called 'transistor effect' was lodged in 1925 by J. E. Lilienfeld [1]. But it took 20 years for the transistors to be demonstrated.

Although the major application of the thin film technology is currently in Liquid Crystal Displays (LCDs), there are many other microelectronic products that could benefit from this technology. For example, the large-area X-ray imager, static random access memory (SRAM) devices, high-density and high-response-speed printer and fax machines.

LCD, using a-Si:H based thin film transistors (TFT) as the switching element in each pixel, is presently the leading technology in the field of flat panel displays.

Plasma Enhanced Chemical Vapour Deposition (PECVD) is the only practical, large area, low temperature, high volume fabrication method which can apply a-Si:H TFT arrays over a large area .

Both a-Si:H and poly-Si thin films are used as semiconductors or active layers in TFTs. The materials often used as a gate insulator within TFTs are silicon nitride (Si_xN_y or shortened SiN), silicon dioxide (SiO_2) or oxynitrides.

Under stress (e.g. gate bias, illumination, radiation) a-Si:H TFTs suffer from instability, as indicated by a shift in the gate threshold voltage. Two possible manifestations of this instability are the creation of midgap states in the a-Si:H channel and possibly the a-Si:H bulk and charge trapping in the gate insulator.

Mainly because the LCD's TFT degradation influences the quality of the display causing the image sticking and flickering, a great amount of research worldwide is devoted to this device reliability.

In the introduction of this thesis, the concept of transistor, the fabrication of a transistor and in particular the case of a-Si:H transistor, the operation of TFT with the emphasis on LCD technology are explained. The problems related to TFTs degradations are briefly introduced here but carefully detailed, analysed and explained in the next chapters.

1.1. Field Effect Transistor

This section explains how the field effect transistor works.

The sources of the history of the transistor are ref [2, 3].

In 1945, Shockley had an idea for making a solid-state device out of semiconductors [2]. He reasoned that a strong electrical field could cause the flow of electricity within a nearby semiconductor. Later, Brattain and Bardeen built the first working transistor, the germanium point-contact transistor. Shockley developed the underlying principle and theory of the junction (sandwich) transistor, which was manufactured for several years afterwards. But in 1960 Bell scientist John Atalla developed a new design based on Shockley's original field-effect theories [3]. By the late 1960s, manufacturers converted from junction type integrated circuits to field effect devices.

Normally, semiconductors do not have many free electrons. Since electric current relies on free charge carriers, the density of current that can travel through pure semiconductor is negligible. Bringing a positively charged metal plate up close will attract negatively charged electrons from semiconductor. These electrons create a pathway (channel) for the current at the semiconductor surface. By controlling the voltage on the metal plate, the current through the semiconductor can easily be switched on and off. Moreover, the current travelling through the semiconductor will be an exact replica of the signal sent to the metal plate. Since this transistor depends on an electric field, it is known as a Field Effect Transistor (FET). Today, most transistors are field-effect transistors. The name 'transistor' is a shortened version of the original term: transfer resistor. Transistors act as either electrical amplifiers or switches [4, 5].

FETs are unipolar devices - only one type of carrier is used in their signal current path. Most FETs have three connections: source, drain and gate. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is the electrode called the source. At the other end of the channel, there is the electrode called the drain. The physical length of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. The conductivity of the FET depends, at any given instant in time, on the electrical diameter of the channel. An insulator layer, usually silicon oxide, separates semiconductor and gate electrode. This is the so-called Metal-Oxide-Semiconductor FET,

MOSFET. A negative voltage applied to the gate electrode attracts electrons to its surface and positive charge carriers or holes are attracted to the interface between the semiconductor and insulator to form an 'accumulation layer'. When a voltage is applied across the source and drain electrodes, a current flows between them. A variation in the voltage applied on the gate influences the current flowing between source and drain.

Field-effect transistors exist in two major classifications. Besides MOSFET there are other transistors known as the Junction FET (JFET) where the gate is made-up by a reverse biased pn junction.

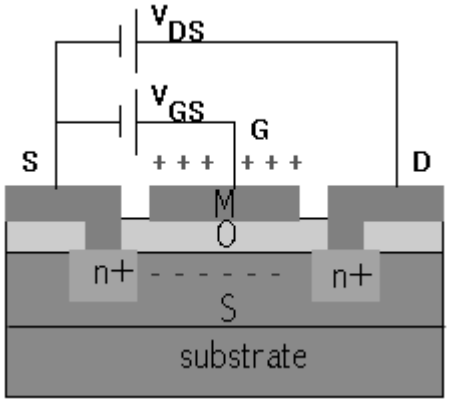

Fig. 1.1. Metal-Oxide-Semiconductor FET; n^+ are source and drain contacts. V_{DS} - drain to source voltage; V_{GS} - gate to source voltage. (http://mediawiley.com/product_data/excerpt)

The MOSFET is constructed from a sandwich of metal, oxide and semiconductor film (fig. 1.1). The oxide in the middle of the sandwich forms a highly insulating gap between the metal of the gate, and the source-drain semiconductor material. The MOSFET can be of enhancement or depletion type. The enhancement device allows virtually no current to flow when the gate-source potential is zero. However, an increase in the gate-source potential (positive for an n-channel device, negative for a p-channel device) attracts opposite charges into the channel region. These allow conduction, so the channel is enhanced and drain-source current increases with increased gate-source potential. The depletion type has some light doping in the channel between source and drain, which allows a channel current to flow even with zero gate - source potential. By varying the gate-source potential in both positive and negative directions, the channel current can be varied.

1.2. Hydrogenated Amorphous Silicon/Silicon Nitride TFTs

This section introduces the device under study in this thesis namely the a-Si:H/SiN TFT.

Hydrogenated amorphous silicon (a-Si:H) is a versatile material with attractive features for a wide range of electronic applications. It can be deposited over large areas at low temperature (< 450 ^{0}C); it has high electrical resistivity when undoped and high conductivity when doped; it creates a good interface with metals, other semiconductors and dielectrics; it is also scratch resistant and non-toxic.

Hydrogenated silicon nitride (a-SiN:H or shortly: SiN) is used as dielectric material for a-Si:H TFTs. A big advantage of using this material is that it can be deposited in the same reactor as a-Si:H, reducing fabrication costs. It is used as the gate dielectric and as passivation layer. When SiN is used as the gate dielectric layer, its capacitance influences the channel current; when it is used as the channel passivation layer, it can affect the off current and the photoleakage current. The deposition process and the sequence of-a-Si:H and SiN deposition influence the interface quality.

Since it influences the electrical parameters of the TFT (field-effect mobility, on/off currents, subthreshold swing, flat-band voltage and threshold voltage), the interface between the a-Si:H and SiN films is of great importance for device reliability. The interface can be affected by many factors: morphology of a-Si:H and SiN films, hydrogen content, a-Si:H density of states, SiN fixed charge.

TFT operation is identical with MOSFET operation for which extensive research has been made and published. However, because the conduction channel is formed in an amorphous material, TFT carrier mobility is much lower than in MOSFET and the threshold voltage is higher. Another difference is that amorphous TFTs work in accumulation whereas MOSFETs work in inversion. The most common a-Si:H/SiN TFT is the n-channel accumulation mode with undoped a-Si:H channel.

a-Si:H TFTs are widely recognized as the most important and successful active devices for use in active matrix liquid crystal display (AM-LCD). TFTs act as a switch in devices like linear sensor arrays, scanner arrays, ink-jet print heads and memory switching devices. Within these applications, hundreds of thousands of TFTs are in constant operation. It is critical that the failure rate for TFTs be minimized within these devices in order to guarantee the reliability demanded by consumer electronics.

Key performance parameters needed to qualify a TFT as a good switching device are: uniformity, stability, low threshold voltage and high mobility.

As a consequence of the demand for low failure rates, the field of reliability physics is a very important discipline acting as a feedback mechanism between the servicing and quality control on one hand and the device design and processing technology on the other hand. In order to investigate TFTs degradation they are artificially 'aged' by accelerated stressing procedures in order to determine potential 'weak points' in their operating life. The procedures can be grouped into the following categories: operation at rated currents and voltages at elevated temperatures, bias stressing, temperature cycling, light and UV radiation exposure, humidity and mechanical stress. The long-term stability of TFTs depends on many different ambient conditions such as: light, radiation, temperature and repetitive duty cycles.

1.3. a-Si:H/SiN TFT Fabrication

This section shows the fabrication flow of an a-Si:H/SiN TFT.

The fabrication process of the TFT starts with the deposition of a-Si:H and SiN on the substrate (glass or c-Si).

Plasma Enhanced Chemical Vapour Deposition, PECVD, is the most used method of depositing thin a-Si:H and SiN films from source gases silane (SiH_4) and ammonia (NH_3), respectively [5].

A big advantage of PECVD in the fabrication of amorphous silicon films is that a-Si:H and SiN deposition is possible over large areas onto many substrates. Moreover, due to the relatively low temperature of deposition, PECVD is a low-cost process compared to a crystalline technology.

In the PECVD process, dissociation of the source gas molecules is stimulated by the coupling of radio frequency (RF) electric field (typically 13.56 MHz) to the charged particles into the reaction chamber (fig. 1.2).

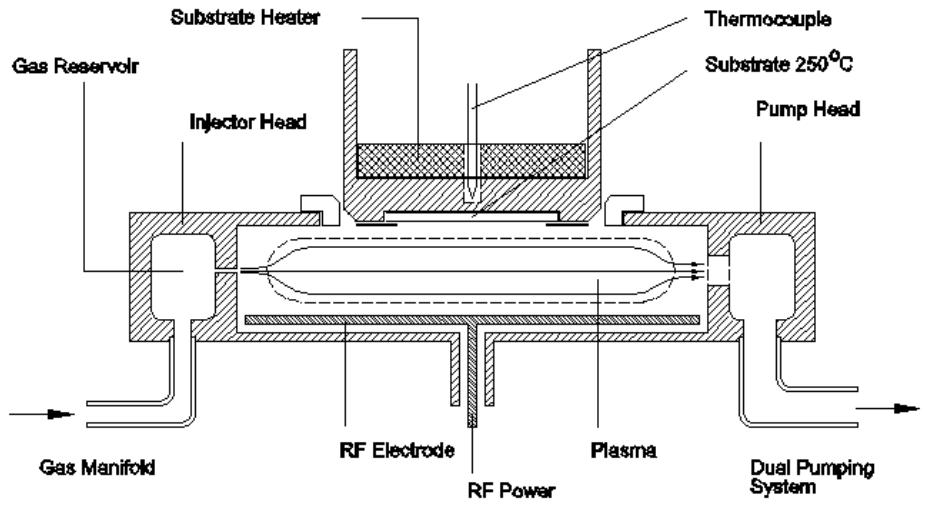

Fig. 1.2. Schematic drawing of PECVD reaction chamber (http://www.imt.fb12.uni-siegen.de/he/forschung/pecvd-e.htm)

Charged species (free electrons and ions) are accelerated by the electric field and collide with molecules of the source gases. In this way, the source gas molecules are excited to higher energy states, primarily by inelastic collisions with the energetic electrons, and dissociate into a variety of radicals, ions, atoms and more free electrons. Radicals and atoms, generated in the plasma, travel to the growing film surface through a diffusion process. Many of these radicals undergo secondary reactions, mainly with parent molecules, during their transport to the substrate. On arrival, they are adsorbed onto the surface where some diffuse on the growing film surface and make chemical bonds at favourable sites to form an amorphous network [6].

TFTs are fabricated in two configurations: bottom gate dielectric and top gate dielectric. In the first configuration, the gate dielectric, SiN is deposited first on the substrate, in the second configuration, a-Si:H is deposited first (fig. 1.3).

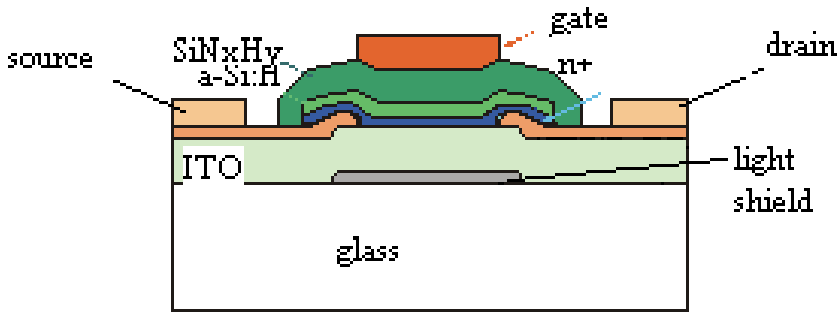

Fig. 1.3. Top gate a-Si:H/SiN TFT for AMLCD application

The a-Si:H as active semiconducting layer and SiN as gate insulator are deposited by PECVD in consecutive runs. The n^+ contacts for source and drain can be deposited also by PECVD (doped plasma), or by a different process (e.g. Implantation Through Mask, ITM). The n^+ layers are necessary to reduce the contact resistance between metal contact of source and drain and a-Si:H. Finally, a metal layer (e.g. Cr, Mo, Al) as gate electrode is evaporated on the insulator layer.

1.4. a-Si:H/SiN TFT Operation

In this section, the operation of a TFT is described. The basic operation of TFTs is identical to that of the Metal-Oxide-Semiconductor-Field-Effect-Transistor, MOSFET.

A positive voltage applied on the gate induces electrons in a-Si:H. At small voltage, these electrons are localized in the deep states of a-Si:H but, above a certain voltage called the threshold voltage, a considerable proportion of the electrons become mobile. Therefore, above threshold voltage the transistor switches on and a current flows between source and drain.

If a negative voltage is applied on the gate, holes accumulate in a-Si:H at the interface with the insulator. The 'hole' channel operation is insignificant because the hole mobility in a-Si:H is two orders of magnitude less than electron mobility and the n^+ contacts cannot supply enough holes to sustain a significant current. However, the 'hole' channel operation is useful in identifying different instability mechanism in device operation. That is why in the study of instability

in a-Si:H/SiN TFTs, ambipolar devices (where 'on-purpose' imperfect metal/semiconductor contacts allow also the conduction of holes) are made and studied [7].

1.5. TFT Applications

Although the major application of the TFT technology is currently in LCDs, there are many other microelectronic products that could benefit from this technology. For example, large-area X-ray imager has been successfully fabricated by integrating n-channel a-Si:H TFTs with p-i-n photodiodes over a glass substrate coated with an X-ray converter material. In this application, the photodiodes are used as transducers and the TFTs as switches to charge the photodiodes [8].

P-channel TFTs have been used to replace high-resistance loads in static random access memory (SRAM) devices, leading to improved cell stability, low standby current, and reduced cell area.

High-density and high-response-speed printer and fax machines have also been successfully fabricated using TFTs.

The TFT can be used as well as chemical sensor, to detect changes in gas-phase hydrogen concentration or liquid-phase potassium concentration.

1.6. Liquid Crystal Displays

The major application of a-Si:H/SiN TFTs is to work as a switch in Liquid Crystal Displays, LCDs. This section explains what are the LCDs and mentions their applications.

Details about the history of liquid crystals, the development and applications of the LCDs are found in ref. [9].

Liquid crystals were first discovered in the late 19th century by the Austrian botanist, Friedrich Reinitzer, and the term 'liquid crystal' itself was coined shortly afterwards by German physicist Otto Lehmann.

In the 1960s it was discovered that placing liquid crystals in an electrical field changes their molecular alignment, and the amount of light that passes through them can be adjusted.

LCDs consist of two plates of glass with a layer of liquid crystal material in between. When an electric field is applied to the cell, the crystals can rotate the plane of polarised light, effectively acting as an on/off switch for the light (fig. 1.4).

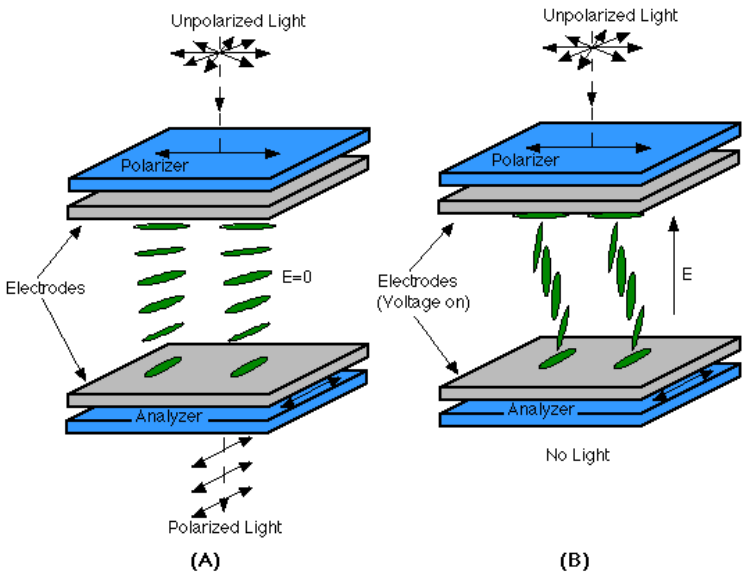

Fig. 1.4. The crystals in an LCD could be alternatively arranged so that light passed the second polarizer when there was no voltage, and not passed when there was a voltage applied between the electrodes (http://www.tu-berlin.de/~insi/ag_heppke/clark/tnlc.htm).

Colour is created by using three cells for each pixel, one for each of the primary colours. Early models were passive, while most new LCDs use an active matrix, which has a TFT behind each element. The transistors control the degree of twist and hence the intensity of the red, green and blue elements of each pixel forming the image on the display.

Until recently, the TFT active semiconductor layer was a-Si:H. These panels have a much higher refresh rate than passive LCDs and are suitable for displaying video as well as still images. There are however a number of problems with this type of display. For instance, creating large active matrix LCD screens is difficult; the larger the screen, the more transistors involved and the more likely some of them are to fail. A very strong light source is required, as the transistors absorb much of the light. Nowadays active LCDs are made with polysilicon rather than a-Si:H. These are much smaller than traditional LCDs, are more transmissive (i.e. brighter) and have higher switching speeds, but are more expensive to produce. Figure 1.5 shows the development of the technology and the corresponding products from 1973 to 2000.

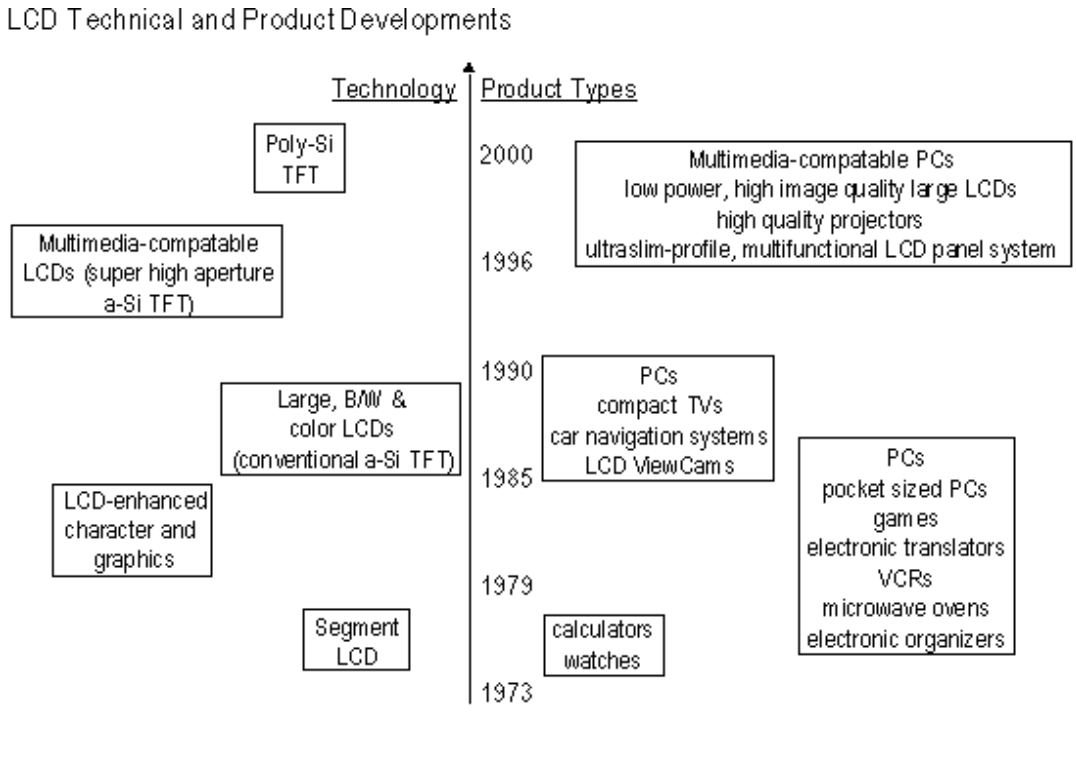

Fig. 1.5. Application of LCDs.

1.7. a-Si:H/SiN TFT degradation

This section refers to the particular case of a-Si:H/SiN TFT stability. The state-of-the art in the degradation issue is described briefly.

After subjecting the TFT to a gate voltage for a certain time, the characteristics of the TFT degrade.

The changes caused by degradation are usually accompanied by a shift of the threshold voltage with little change in mobility. Two separate mechanisms have been found to contribute to this effect. One is charge trapping in the SiN. The second one comes from the changes in the a-Si:H density of states. In the mechanism based on the charge trapping, the transfer of charge from the a-Si:H channel into the SiN defect states is considered to occur. In the mechanism based on defect creation, the weak bonds in a-Si:H break to form two dangling bonds. These two dangling bonds are prevented from recombination by a hydrogen atom that moves to one of the two defect sites.

It is difficult to distinguish on a particular mechanism because both can simultaneously occur depending on the gate voltage, ambient temperature and quality of a-Si:H and SiN films.

This thesis studies the bias stress induced TFT degradation. It contributes to the understanding of the degradation phenomena and the effects on the TFT stability. Based on the experimental evidence, the thesis proposes solutions to improve the TFT electrical stability.

The limited stability of the device due to electrical characteristic degradation is not crucial for the utilization of a-Si:H TFTs in LCDs. This is due to the small duty cycles the TFT undergoes in this application and the slow TFT degradation comparing with the final product lifetime. However, using the TFT for the column-raw driver circuits for example requires a high stability. Therefore more stable Complementary Metal Oxide Silicon TFT, CMOS-TFT, is preferred for the drivers. However, the large amount of interconnects and the attachment of the dies to the glass substrate complicates the circuitry reducing the reliability and increasing the production costs. The implementation of a highly reliable TFT, instead of CMOS in such application would decrease considerably the production costs.

1.8. Thesis summary

The electrical degradation of a-Si:H/SiN TFTs is the subject of this thesis.

The thesis is organized in chapters starting with an introduction in chapter 1, a brief presentation of the a-Si:H and SiN points of interest together with an electrical and physical characterization of as-deposited films in chapter 2.

Chapter 3 describes DUT fabrication, characterization and theoretical modelling of the device operation.

In chapter 4**,** the theoretical background for the existing models describing the a-Si:H/SiN degradation is presented.

Chapter 5 describes the degradation of threshold voltage, flat band voltage and subthreshold swing due to gate bias stressing at room temperature of a-Si:H/SiN TFTs. The threshold voltage, flat band voltage and subthreshold slope obtained by current - voltage and capacitance - voltage measurements are measured and correlated each other.

In chapter 6, a new testing method of accelerated gate bias degradation by measuring drain current transients at selected time intervals is presented. The results were interpreted according to the tunnelling front model and defect creation model. A 'hybrid' model to explain the a-Si:H/SiN TFTs behaviour during alternative and repetitive cycles of stress at different gate biases and ambient temperature is proposed.

To characterize the interface of a-Si:H/SiN films we used Charge Deep Level Transient Spectroscopy, QDLTS, and Slow Trap Profiling, STP, methods of investigation. The results of QDLTS and STP investigation are described in chapter 7.

In the annexe**,** the experimental techniques used for device characterization are presented.

At the end of this thesis, a summary of the research is presented.

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CHAPTER 2

AMORPHOUS SILICON AND SILICON NITRIDE THIN FILMS

This chapter describes the differences between crystalline silicon and amorphous silicon and refers to the improvement of amorphous silicon properties when hydrogenated. The effect of nitridation and hydrogenation of amorphous silicon is described as well.

The defect in amorphous hydrogenated silicon is presented in the light of defect-pool model. The structure, chemical composition and electronic profile of the interface between amorphous silicon and silicon nitride are described briefly.

The a-Si:H and SiN films deposition together with a physical and electrical characterisation of films is shown.

2.1. Crystalline and amorphous silicon

A crystal is defined as a three dimensional repetitive structure of atoms. Over a long distance one can record the same pattern of spatial arrangement within the atoms. In crystalline silicon, the silicon, Si atoms are covalently bonded with 4 neighbours in tetrahedral directions forming a diamond-like structure.

The length of Si-Si bond is the same over the entire network of atoms [1].

Crystalline Si has sharply defined electron energy bands: the valence band is fully occupied and the conduction band is empty at 0 K. The transition of electrons across the energy gap is due to thermal and/or optical excitation.

The structural randomness of amorphous solids lacks long-range order while short-range order is adequately maintained. The atoms are arranged in an open network with correlation in ordering only up to the third or fourth nearest neighbours.

A characteristic feature of amorphous silicon (a-Si) is the disorder-induced localization of states near the band edges and band-gap defects formed in the network resulting from internal tension or deposition conditions (fig. 2.1). The

fluctuation in the length of covalent Si-Si bond and the angle between the bonds lead to an abundance of *band tail* states decaying exponentially from the band edges [2].

The disorder leads to localisation of electron wave functions associated with some covalent bonds. Because these bonds can be easily broken they are called *weak bonds* (WB).

By radiation exposure or electrical stress, the WBs break resulting in under-coordination (3 instead of 4 covalent bonds) defects so called *dangling bonds* (DB) [1-4]. The DBs are generated at high temperature (> 420 K) in thermal equilibrium with the occupancy of tail states and they are preserved by quenching the film to low temperatures (< 420 K) [1, 2].

The electronic properties of amorphous films depend on the density and energy distribution of the localized gap states. Experimental study obtained by Electron Spectroscopy Resonance (ESR), Optical Spectroscopy (OS), and Space Charge Spectroscopy (SCS) contributed to the present knowledge of the distribution of gap defects [1].

The DB deep states lie in the a-Si band gap. DBs resulting from breaking of WBs, tail and gap states resulting from the disorder, all act like traps, limiting the mobility.

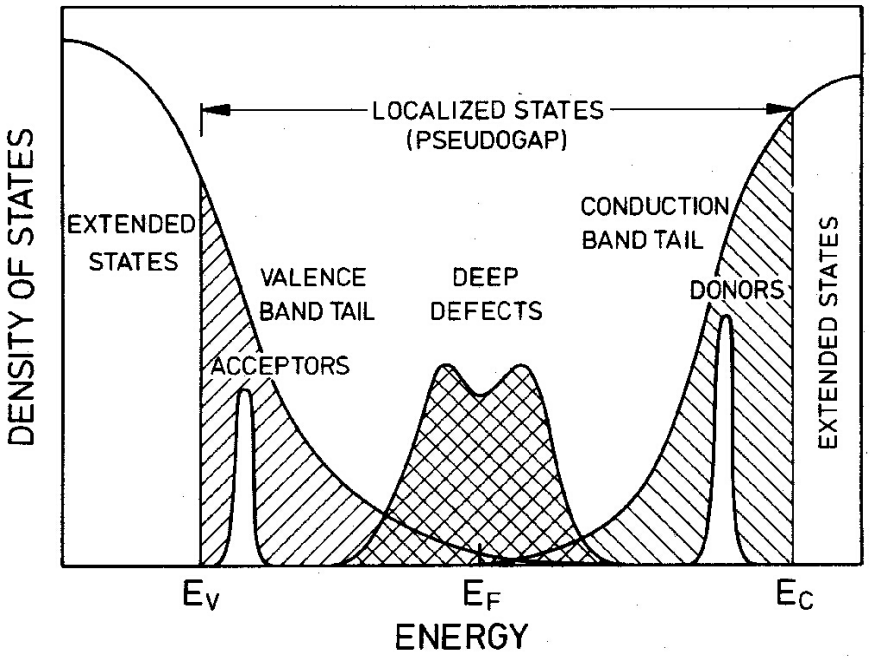

Fig 2.1. Representation of a-Si band gap states [1].

In pure crystalline Si, the Fermi level is situated in the middle of the band gap and impurity doping influences its position. In intrinsic a-Si, the Fermi level is almost fixed a little bit above the middle of the band gap due to high density of DBs.

2.2. The particular case of hydrogenated amorphous silicon and hydrogenated silicon nitride

Hydrogenation of a-Si results in so called a-Si:H or a-SiH_x.

The a-Si:H can be used for a variety of applications such as Photovoltaics, Thin Film Light Emitting Diodes, TFLED, Photosensors, Electrophotographics and Thin Film Transistors, TFT. Among these applications, photovoltaics and TFTs are the areas where a-Si:H based materials have a leading role. The unique advantages of a-Si:H thin films are high light absorption (40 times higher than that of c-Si), low temperature for deposition (< 250 °C) and low cost substrates (glass, metals and plastics).

When a-Si:H is prepared by decomposition of silane (SiH_4) in RF plasma, PECVD, at high temperature, the hydrogenation (10 – 15 % H in a-Si:H bulk according to Fourier Transform Infrared Spectroscopy, FTIR [1]) the density of states, DOS, in the gap of a-Si lowers from 10^{20} to 10^{15} $cm^{-3}eV^{-1}$. Other hydrogenation techniques such as reactive sputtering in Ar-H mixtures and post-hydrogenation from silanes have been proposed, but plasma deposition leads to the best results and is widely used in industry.

Due to the low density of DBs after hydrogenation, the Fermi level in a-Si:H films can easily be moved by doping, exposure to radiation or biasing.

The value of the band gap energy of a-Si:H, varies from 1.7 eV to 1.8 eV depending on the percentage of H in the film.

Despite the fact that the H presence enhances the electronic properties of the material, in larger concentrations it can degrade the mechanical properties, reducing for example, the hardness of the material. It is believed that many of the metastability effects in a-Si:H are related to the presence of hydrogen [5]. Therefore, the H percentage is very important for good-quality a-Si:H films.

Nitridation and hydrogenation of a-Si resulted in so-called silicon nitride (SiN or a-SiN_xH_y) that shares the same class of amorphous silicon alloys as a-Si:H.

PECVD deposition from silane, ammonia NH_3 (and nitrogen N_2) results in so called a-SiN:H or SiN_xH_y. The synthesis conditions determine the ratio (x) of N/Si from Rutherford BackScattering, RBS, to be from 0.5 to 1.6 [6]. When $x = 1.3$, SiN is stoichiometric whereas for $x < 1.3$ SiN is called sub-stoichiometric or Si rich SiN and for $x > 1.3$ SiN is called above-stoichiometric or N rich SiN. For low N contents or Si rich SiN, H prefers to bind to Si and for high N contents or N rich SiN this chemical preference switches [7].

The percentage of H in a-SiN:H is between 15 and 30 % according to FTIR studies [1]. In the as-deposited samples, H forms chemical bonds with both Si and N, where it determines most chemical (stoichiometry), physical (band gap energy $5\ eV < E_g < 7\ eV$) and electro-physical properties of a-SiN:H.

2.3. Weak and dangling bonds in a-Si:H

Undoped a-Si:H is modelled by exponential band tails with characteristic slopes for each band. Constant photocurrent measurement CPM showed that the a-Si:H valence band has a larger slope than the conduction band with characteristic energies of 50 meV (Urbach tail) for valence band and 25 meV for conduction band [1].

The conduction band and valence band tail states are spatially correlated [8]. That means that a broadening of valence band tail matches with a broadening of conduction band tail. The conduction band tail slope is very important because the conduction band tail controls the field-effect mobility of TFTs. The valence band tail slope is important because the WBs are situated there, hence the distribution of energy barrier the WBs overcome in order to form DBs is proportional to the Urbach energy [1]. It is still in debate whether the valence band tail states are associated with stretched bonds, but it is clear that the disordered nature of a-Si:H is responsible for the existence of the band tails [9].

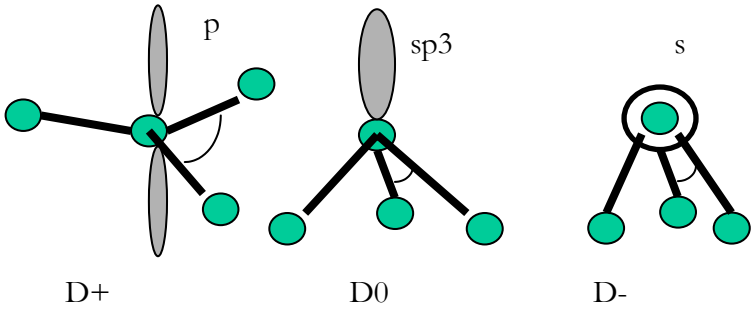

Fig. 2.2. The orbital configurations of the dangling bonds in a-Si:H

In addition to the WBs, the a-Si:H network contains a large number of amphoteric DBs with states situated in the band gap of a-Si:H [4]. Amphoteric means that, according to the Pauli principle, in a defect orbital one can find 1, 2 or no electrons corresponding to D^0 (neutral), D^- (negative), or D^+ (positive) states of the defect (fig. 2.2 right).

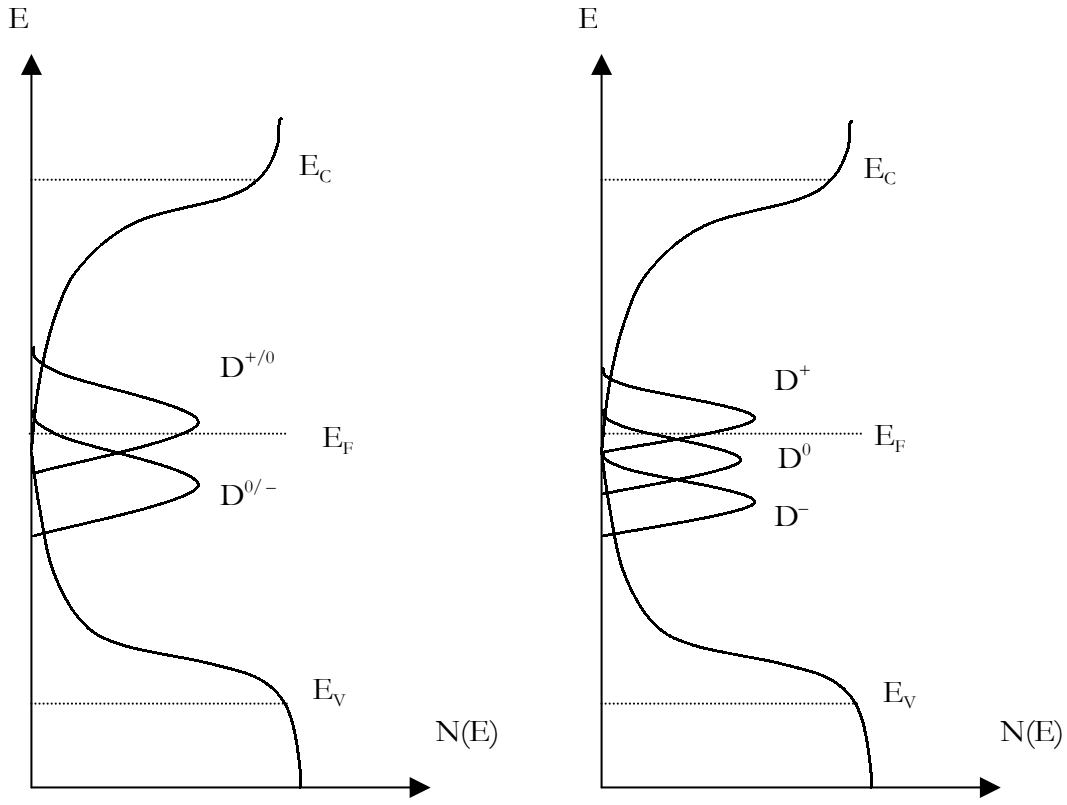

Fig. 2.3. The intrinsic a-Si:H DOS. Transition levels between defects (left) and defect representation in the band gap (right).

Maximum two electrons can occupy a DB. Thus, for each DB there are 2 transition levels: the transition level with energy E_d caused by bringing an electron to an empty DB (donor $D^{+/0}$ first transition level) and the transition level with energy $E_d + U$ caused by bringing an electron to a singly occupied DB (acceptor $D^{0/-}$ second transition level) (fig. 2.2 left). E_d is referred to as defect energy and U is the negative correlation energy caused by a coulombian repulsive force between the 2 electrons that can occupy a DB [10] (fig. 2.3).

The defect pool model describes the defect density of states under thermal equilibrium. According to this model a pool of potential DBs, originating in WBs [11], extends across the entire a-Si:H band gap. Bar-Jam pointed out that the formation energy of a defect depends on its charge state and, moreover, that the difference in the formation energies of the defects depends on the Fermi level energy and the energy of the defect itself [12]. Winer defined the terms of the modern defect pool model assuming that DOS was dominated by defects of only one charge type in each material (negative in n type, positive in p type and neutral in intrinsic) [13, 14]. Schumm and Bauer corrected this assumption by taking into account the simultaneous creation of DBs in all charged states [15].

When the Fermi level shifts (e.g. by applying bias stress) towards either of the energy bands the occupancy of D^0 is changed to D^- or D^+ (e.g. when Fermi level moves towards the CONDUCTION BAND the D^0 changes to D^-). Charged DBs act like traps for carriers of opposite charge influencing the amount of mobile carriers in a-Si:H. The energy distribution of amphoteric defects is modelled gaussian-like.

2.4. Interface between a-Si:H and a-SiN:H

The interface between the semiconductor and the insulator is of high importance for all electrical characteristics and reliability of TFT devices. In the literature, the main issues in studying a-Si:H/SiN interface are:

1. *structure;*
2. *profile*;
3. *electronic states*.

In respect to the first issue the debate is on the sharpness of the interface (abrupt or gradual), the extent of the interface and the influence of deposition conditions. With respect to the second issue, many papers show that the interface density of states depends on the order of deposition of semiconductor and insulator [16] and on the quality and stoichiometry of the insulator [17].

1. *Structure*. Transmission Electron Microscopy (TEM) on a-Si:H/SiN interfaces indicate that relatively smooth and uniform interfaces of amorphous materials are obtained by PECVD deposition of a-Si:H on top of SiN. The interface spans beyond the crystallographic separation between semiconductor and insulator to transitional regions or 'defected' regions caused by lattice mismatch [16]. Accordingly, the interface extends onto both sides of the crystallographic interface and consists of weak Si-Si bonds and different types of vacancies. The vacancies are located in a region a few atomic layers from the crystallographic interface and change their density under stress conditions. Those traps are *interface traps*. All experiments performed thus far are consistent with an interfacial layer width being dependent on the order of deposition of a-Si:H and SiN. When a-Si:H is deposited on SiN, TEM shows the presence of an N-tail carried over 10 Å into a-Si:H and when SiN is deposited on a-Si:H a damaged layer due to the N-ions bombardment extends over a distance of 35 Å into the a-Si:H [18].

2. P*rofile*. As demonstrated by different techniques such as photoelectron spectroscopy, scanning tunnelling microscopy and infrared ellipsometry, between a-Si:H and SiN is an abrupt, highly hydrogenated interface [19, 20]. The hydrogen is immobile at very low temperature but at intermediate temperature it starts to diffuse allowing defect equilibration [21]. The interface width is between 3 Å and 10 Å when a-Si:H is deposited on SiN and 17 Å to 20 Å (some authors

reported even 35 Å) when SiN is deposited on a-Si:H. The larger interface width when SiN is deposited on a-Si:H is caused by nitridation of a-Si:H during SiN deposition.

3. *Electronic states*. In the sections above we have briefly characterized the defects (or traps) from the point of view of their position in the band gap of either a-Si:H or SiN. The language used to describe the *defects* from an electrical response point of view names them *states* and from the structure and location point of view it names them *traps*. The traps are not only DBs but also vacancies or impurity defects. Unfortunately, it is difficult to distinguish one type of physical defect from another based solely on electrical data [22]. That is why an inappropriate nomenclature creates confusion when trying to compare the results in the literature: similar defects are identified by different names or different defects by the same name.

In this thesis, defects are called traps when discussing about their influence on the device electrical parameters. With respect to their position from the interface, the traps are either bulk semiconductor or bulk insulator traps, either interface traps or border traps. With respect to their electrical response to external stimuli, the traps are called states. There are fixed states or deep states, interface states or switching states, respectively [23].

Also in this thesis the traps are called either *fast* or *slow* traps with respect to their electrical response. Many papers classify the traps in the insulator as slow states and the traps at the crystallographic interface as fast. Focusing on this problem, some authors pointed out that so called border traps that are located in the interface on the SiN side do exchange charge with the a-Si:H on a fast time scale (< 1 s) and that is why they cannot be considered bulk SiN traps. They have been called *border traps* or *switching states* [24]. The methods to discriminate between true SiN bulk states and the switching states are diverse: C–V hysteresis, 1/f noise, and Slow Trap Profiling (STP) [25] that will be used in characterization of the devices presented in this work.

The role of interface states on the calculated TFT characteristics is well documented. It has been shown (e.g. by measurements on dual-gate devices) that the charge transfer within the states near the interface causes band bending and electron accumulation in a-Si:H [26]. The accumulated charge density depends on the deposition order. This dependency is much higher for top nitride than for bottom nitride but it is not affected by the interface composition [18]. In spite of much research on the interface states it is still a challenge to discriminate between bulk states in a-Si:H and true interface states. Several methods have

been proposed: transient photocurrent, transient voltage, transient photocapacitance, quasistatic C–V, and charge - Deep Level Transient Spectroscopy (QDLTS) [27, 28]. The last two methods will be used for characterization of our devices.

2.5. Deposition of a-Si:H and a-SiN:H films

The parallel-plate PECVD (Plasma Enhanced Chemical Vapour Deposition Electrotech 8000) system has been used for experiments on deposition of a-Si:H and SiN_xH_y films.

Both a-Si:H and SiN samples were deposited by PECVD in the same reactor chamber, without breaking the vacuum. The source gas was a mixture of 2 % SiH_4 in Ar. The substrate temperature was 250 ˚C, the discharge frequency set to 13.56 MHz and the source gas flow was fixed at 2000 sccm for all samples. SiN was deposited from (2 %) SiH_4/Ar with NH_3 and N_2 gases. NH_3 flow was 37 sccm for all SiN depositions.

It has been reported that the characteristics of a-Si:H and SiN films depend on plasma power [29, 30]. Two regimes have been identified for RF plasma deposition of a-Si:H: so called α-regime at low deposition rates and γ-regime at high deposition rates. In the γ-regime the a-Si:H films contains micro crystals because the hydrogen preferentially etches the amorphous phase of the film leaving behind a higher fraction of crystalline phase. The plasma power is a very important key-factor in the deposition of SiN as well. Above a critical level the plasma induces gas-phase reactions to particles and below a critical level it does not produce ammonia activation [31].

The plasma power level has been set at 60 W and 100 W respectively for two depositions of a-Si:H and SiN films. The N_2 flow for SiN depositions was set at 1500 sccm and 2000 sccm respectively.

The depositions aimed to 'true' (without crystalline islands) amorphous α a-SiH and SiN with low trap density.

The deposition parameters that vary during deposition of a-Si:H or SiN are listed in the table 2.1.

samples	Power [W]	Pressure [mtorr]	N_2 [sccm]
SiN(1)	100	850	1500
SiN(2)	60	850	1500
SiN(3)	60	985	2000
SiN(4)	100	985	2000
a-Si:H(1)	60	650	-
a-Si:H(2)	100	650	-

Table 2.1. Parameters of PECVD deposition for a-Si:H and SiN samples.

2.6. Physical characterization of deposited a-Si:H and SiN films

The thickness of a-Si:H and SiN layers were both measured by the Surface Profiler Sloan (Dektak 3030 within 5 % error) to be about 250 nm a-Si:H film and 300 nm SiN film.

The way in which X ray diffraction, FTIR and RBS measurements have been performed and the equipment used is explained in Annexe.

The structural characterization of a-Si:H, particularly with regard to crystallization and hydrogen-related bonds had been performed by means of FTIR and XRD.

The samples of a-Si:H were studied by the means of X ray diffraction. The a-Si:H deposited at 60 W and 100 W were both fully amorphous (fig. 2.4) but some small clusters appear in a-Si:H deposited at 60 W and not in the sample deposited at 100 W. The origin of the cluster peak may be related to the existence of open-volume defects resembling silicon vacancies. These structural in-homogeneities are reported to appear in PECVD deposited materials and they are most probably related to the spatial variation of the bonded hydrogen [32, 33].

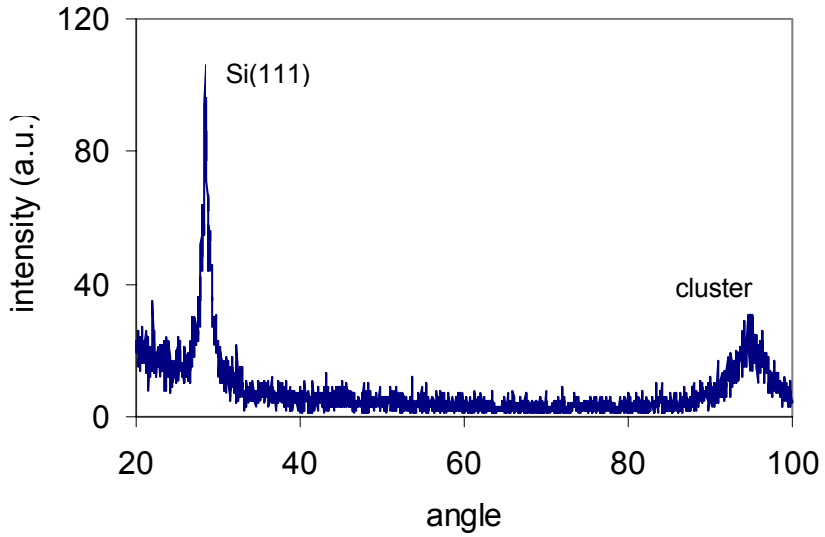

Fig. 2.4. XRD spectrum of a-Si:H sample deposited at 60W. The emergent c-Si diffraction peak around 30° and the 'cluster' peak around 95° are indicated.

FTIR spectra of a-Si:H films present a wagging SiH mode at 640 cm^{-1}, a bending SiH_2 mode at 840-890 cm^{-1} and a stretching SiH mode at 2000 cm^{-1}. The H is primarily bonded in a monohydride (SiH) configuration and the percentage can be calculated either from SiH rocking mode at 630 cm^{-1} or from SiH stretching at 2000 cm^{-1} (fig. 2.5) [34]. The dihydride mode appears as a broad peak in low quality γ a-Si:H [35] and only as small shoulder in our samples therefore the deposited material is α a-Si:H. When deposited at 100 W, the wagging mode peak is broader but not higher and the dihydride peak is smaller than at deposition power of 60 W. Some authors reported that the existence of high hydrides' peak is an indication of network relaxation in a-Si:H and, instead of showing a bad quality of a-Si:H, it indicates less voids in a-Si:H [36]. From the integrated absorption peak of the wagging mode and using a proportionality factor of $2 \cdot 10^{19}$ cm^{-2}, the H content is estimated to be about 14 % for sample 1 and 16 % respectively for sample 2 [34].

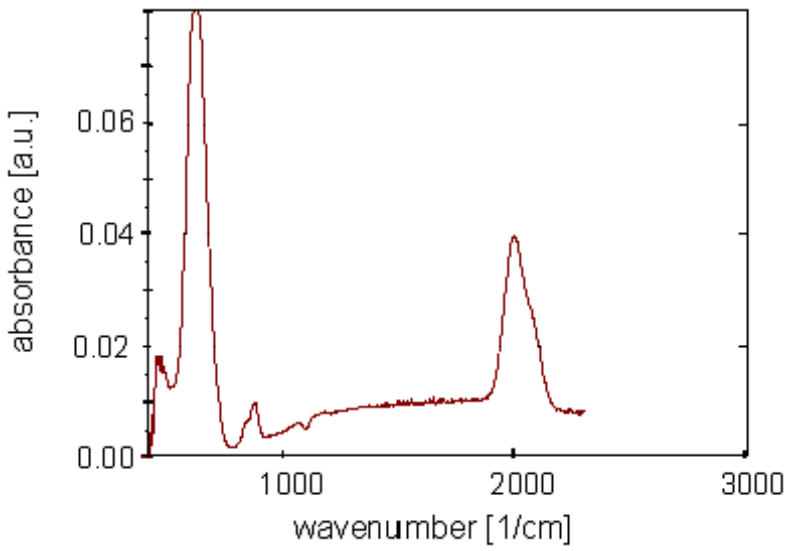

Fig. 2.5. Infrared absorption spectrum for a-Si:H deposited at 60W.

SiN_x layers were studied by FTIR and RBS method in order to know the atomic bonding, H percentage in SiN and stoichiometry (N/Si ratio).

The absorption peaks in FTIR spectra (fig. 2.6) are attributed to SiN bending mode at 850 cm^{-1}, NH_2 bending at 1500 cm^{-1}, SiH stretching mode at 2100 cm^{-1} and NH stretching at 3350 cm^{-1}. H content was evaluated by integrated absorbance under the peaks at 2100 cm^{-1} and 3350 cm^{-1} using calibration (proportionality) factor of $1.4 \cdot 10^{20}$ cm^{-2} and $2.8 \cdot 10^{20}$ cm^{-2} [37, 38].

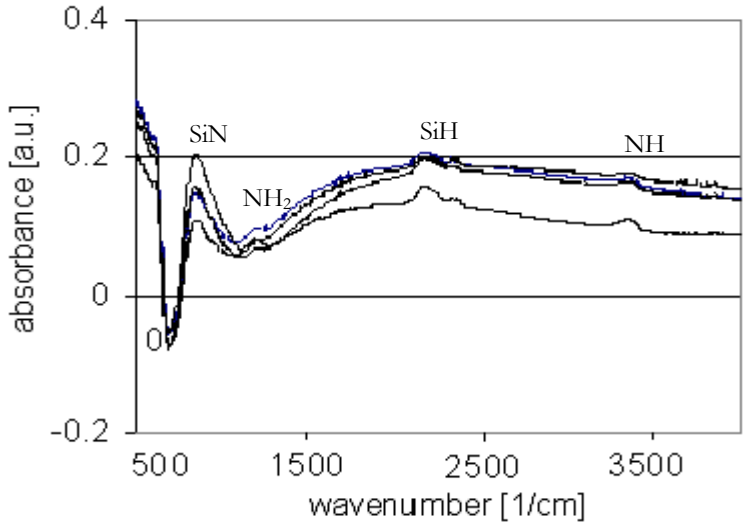

Fig. 2.6. Infrared absorption spectra of all deposited SiN samples.

A concentration range for bonded H between 17 and 23 % in SiN samples was calculated.

RBS (fig. 2.7) has been used to determine the atomic composition (x) of SiN_x. N/Si ratio has been evaluated comparing the experimental data with a simulated spectrum.

It appeared that the deposited SiN_x is below stoichiometric $SiN_{1.33}$ (x = 1.33). It is known that N/Si ratio depends on the gas phase composition and Si-rich films are easily formed by PECVD deposition because excess Si atoms exist mainly in the form of poly-silane in the gas phase of plasma decomposition [39]. Close to stoichiometry is sample 4 that is deposited at 100 W with 2000 sccm N_2. Increase of plasma power causes an increase in N/Si ratio due to increase of NH_3 dissociation. However, the increase of N/Si ratio in sample 4 is bigger comparing to sample 1 that is deposited at 100 W; this is mainly due to increasing of N_2 flow. It appears that excess of N_2 in plasma favours the formation of stable NH and/or NH_2 bonds in disfavour of less stable SiH bonds that easily loose the H atom to form DBs.

The complete results of RBS and FTIR are shown in table 2.2.

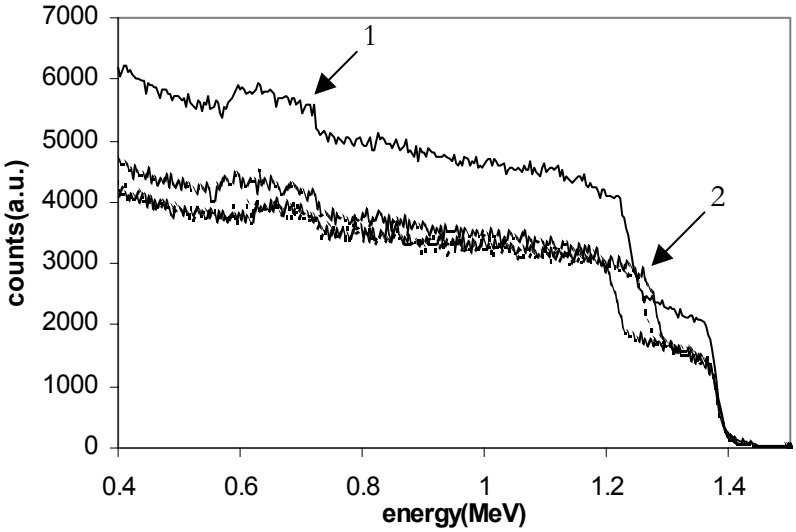

Fig. 2.7. RBS spectra of all deposited TFTs. 1: He ions backscattered from SiN; 2: He ions backscattered from a-Si:H.

The ellipsometry (Plasmos Ellipsometer SD 2002) provided the value of SiN refractive index. The values are within a narrow range for both deposition

powers used (table 2.2). A refractive index around 1.9 is characteristic for SiN with low charge trapping sites [31].

SiN sample	Refraction index	% H bonded	N/Si ratio
1	1.92	23.5	1
2	1.86	21.3	0.78
3	1.88	17.2	0.96
4	1.96	20.1	1.26

Table 2.2. Physical and chemical parameters of as-deposited SiN films

2.7. Electrical characterization of SiN films

The presence of fixed charges in SiN, close to the a-Si:H/SiN interface, leads to band bending at the interface. The interface characteristics (e.g. interface states, chemical composition, sharpness, etc.) influence most of the important transistor characteristics (on/off current, mobility and threshold voltage). Therefore, when discussing the influence of the a-Si:H deposition process on TFT characteristics, the dielectric properties of the gate insulator cannot be neglected.

The electrical behaviour of silicon nitride has been studied using a Metal-Insulator-Semiconductor, MIS configuration for Si rich and nearly stoichiometric SiN films described in section 2.5.

SiN films with 300 nm thicknesses were deposited on c-Si substrate ([111] orientation; resistivity 10 Ωcm, n-type doping ~ 10^{15} cm^{-3}). Before loading the substrate into the deposition chamber, they had been cleaned including rising in dilute hydrofluoric (HF) acid to remove any silicon oxide on the silicon surface. Aluminium was evaporated onto the back surface of the substrate in order to form ohmic back-contacts.

The high-frequency capacitance of MIS structures was measured by superimposing an a.c. signal with the frequency of 10 kHz on a ramped d.c. bias between the top contact and the substrate. The high-frequency capacitance was

measured with a Hewlett-Packard 4275A multi-frequency meter. When there was no a.c. signal applied, but only a d.c. bias with a sweep rate of 0.1 V/s, the quasistatic C–V curve was measured with a Hewlett-Packard 4140B pA meter. The measurements had been done using a Karl Suss PM8 Probe Station (Hg probe $0.53\ mm^2$ for top contact).

From the frequency independent insulator capacitance in accumulation, the dielectric constant had been found to be within a narrow range of values around 5.8 (table 2.3), slightly lower for sample 3.

SiN sample	Dielectric constant	$-V_{th}[V]$	$-V_{fb}[V]$
1	5.85	23.6	22.2
2	5.77	20.5	20.5
3	5.58	18.2	17.2
4	5.65	18.4	17.3

Table 2.3. Electrical parameters of deposited SiN films

Quasistatic and high-frequency C–V measurements of Al/c-Si/SiN structures show a large flat-band voltage V_{fb} and a large threshold voltage V_{th}. The interface state density was calculated from the high frequency characteristics using Terman's method [40]. The origin of the interface states is assumed to be the Si amphoteric DBs and the density is expected to increase with the increase in the Si content in the SiN film [41, 42]. The threshold and flat-band voltage values (V_{th} and, respectively, V_{fb}) decrease from –24 V in sample 1 to –18 V in sample 3 and, respectively, from –22 V to –17 V from sample 1 to sample 3 and 4 (table 2.3). The high values of threshold and flatband voltages in our samples are consistent with a large density of states at the interface Si/SiN in Si-rich SiN films [43]. Among the measurements, lower V_{th} and V_{fb} values were measured for samples 3 and 4 where N_2 flow for nitride deposition was higher and the percentage of bonded H was lower comparing to samples 1 and 2 (and irrespective to the deposition power).

2.8. Conclusion

The a-Si:H for both 60 and 100 W deposition powers is amorphous. Due to low silane dilution the increase in power did not result in poly-crystalline grains inside a-Si:H. Because of absence of a prominent dihydride peak in FTIR spectra, it was concluded that the a-Si:H was deposited in α regime. However, measurements of XRD showed that open volume defects clustered when the deposition power was set to 100 W. The origin of the clustered defects is the Si dangling bond.

All as-deposited SiN films are below stoichiometric (sample 4 is the closest to Si_3N_4). It has been proven that devices deposited at high N_2 flow are closer to the stoichiometry that the others. It appears that the samples deposited at high N_2 flow have slightly less interface states and fixed insulator charge than the samples deposited at low N_2 flow and in this respect the nitride obtained with this recipe is better than the other samples presented in this chapter. Therefore increasing of N_2 flow is the solution in obtaining stoichiometric and N-rich SiN.

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CHAPTER 3

THIN FILM TRANSISTORS

This chapter briefly presents the state-of-the art in the field of the a-Si:H metastability. The metastability of a-Si:H is in strong relationship with a-Si:H TFTs degradation. There are described the theoretical models in the literature regarding degradation of a-Si:H TFTs, focusing the attention on those characteristics that make the distinction between the models. Experimental threshold voltage shift obtained by stressing TFTs is fitted using the models described in this chapter.

3.1. Device fabrication

Many configurations of TFTs have been described in the literature; the most common are the inverted staggered and staggered structures. The inverted staggered structure (fig. 3.1) is more popular than the staggered structure because the a-Si:H layer is deposited after SiN_xH_y which results in a lower interfacial density of states between the gate dielectric and the a-Si:H layer [1].

The devices presented in this work are the inverted-staggered tri-layer structure as shown in fig. 3.1.

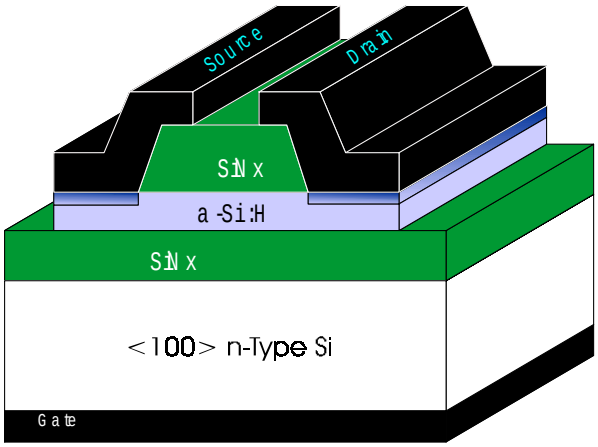

Fig. 3.1. Cross-section of inverted staggered a-Si:H/SiN TFT

The process flow of the inverted staggered TFT is shown in fig. 3. 2.

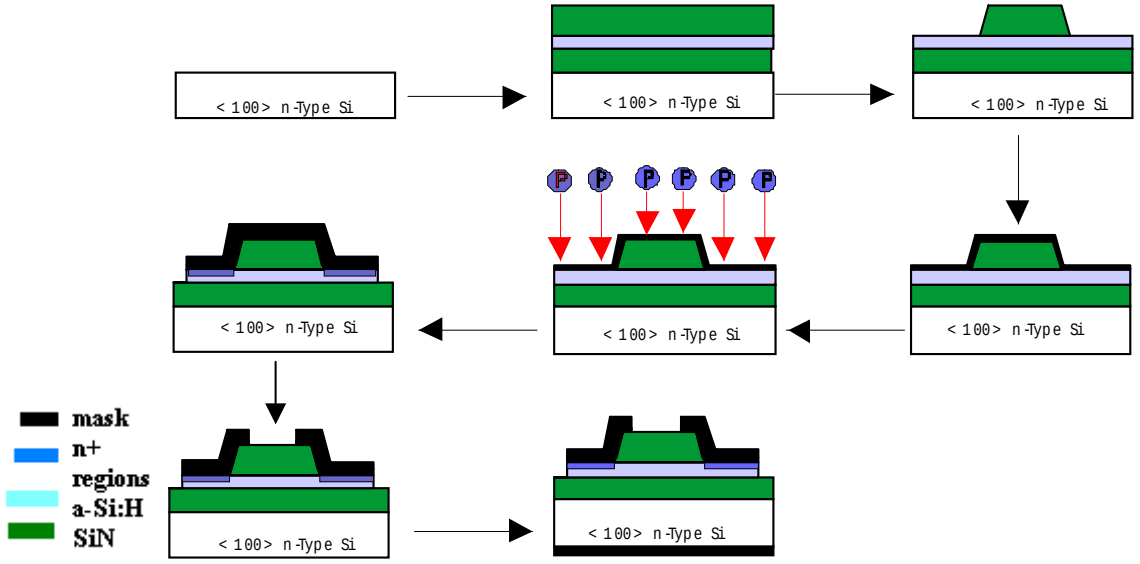

Fig. 3.2. Fabrication process flow.

After standard cleaning of the silicon substrates, 250 nm of silicon nitride and 300 nm of hydrogenated amorphous silicon films were deposited on the silicon substrate (used as common gate) without breaking the vacuum. The deposition parameters are discussed in 2.4 and listed for each sample in table 1 of chapter 2. Devices have W = 40 – 500 μm and L = 20 – 100 μm with all combinations either W/L = 500/100 or W/L = 40/20.

Subsequently, another 100 nm silicon nitride layer was deposited as a passivation layer. The passivation layer is used as a mask for the ion implantation process. First mask removes the passivation SiN_xH_y layer from everywhere on the substrate except from the area, which will be the layer to protect the channel. This mask defines the gate length. A wet BHF etching at room temperature is used to etch the nitride. After the first run, a thin metal layer of 10 nm Mo, which is used as scattering layer, is deposited by DC sputtering. Ion implantation through metal films (ITM) has been used to form ohmic contacts for source and drain. The implantation of phosphorus atoms (to define n^+ regions for source and drain) through the scattering layer is carried out with ion energy of 40 keV and doses of $3 \cdot 9^{15}$ ions/cm^{-2}. The scattering layer was not removed after the ion implantation. To obtain a reduced resistivity, a second metal layer of 200 nm Mo is deposited on top of the thin scattering layer to define source and drain contacts.

The second mask is used to define the active area for TFT devices. This mask removes the metal layer and a-Si:H layer everywhere except from the TFT area. The metal layer is patterned by wet etching. After patterning of the metal layer, the a-Si:H layer is etched by using the same photoresist.

A wet H_3PO_4:HNO_3:HF (volume rate of 60:5:1) etchant is used to etch the a-Si:H layer. The third mask is used to form source and drain regions by removing the metal layer on top of passivation layer. The bonding pads are formed by MoCr sputtering. Finally, an Al layer is deposited by DC sputtering on the backside of the substrate. For dopant activation, the devices are annealed in dry nitrogen at 280 ^{o}C for 1 hour.

3.2. Device characterization

In this section, the mobility, threshold and flatband voltages for the transistors labelled as TFT 1-4 in table 3.1. The semiconductor and insulator films for each TFT had been described and characterized in chapter 2.

The values of the field effect mobility and threshold voltages for TFTs were then extracted from the slope and intercept of the I_d–V_g characteristic (fig. 3.3). The values of the flat band voltage have been extracted from C–V measurements of MIAS capacitors deposited in the same wafer as the TFTs (fig. 3.4). I–V and C–V measurements on TFTs together with the way in which mobility, threshold voltage and flatband voltage are calculated from the measurements, are described in the Annexe.

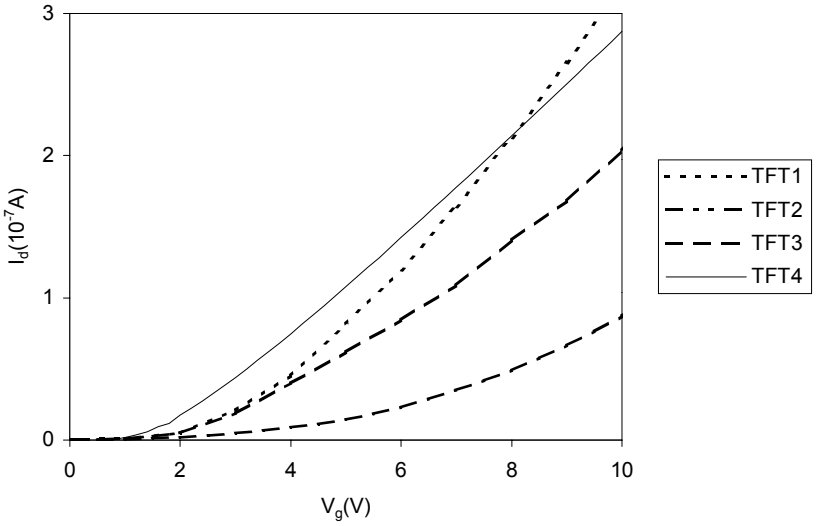

Fig. 3.3. Transfer characteristics of four devices W/L = 5) for $V_d = 0.5$ V.

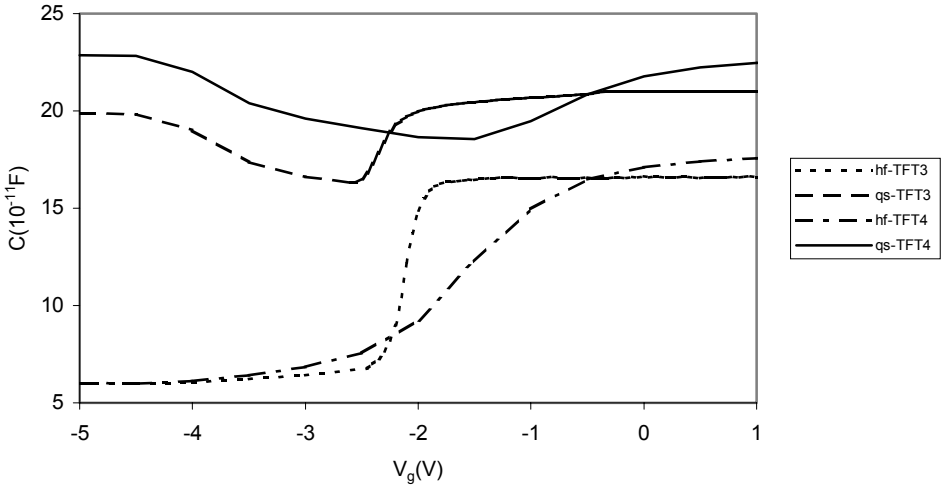

Fig. 3.4. Capacitance versus gate bias of two MIAS capacitors. ($A = 0.01$ cm^2)

A statistic of the results show homogeneous values of field-effect mobility, μ in the range of 0.1 – 0.3 cm^2/V·s and a spread in the values of threshold voltage, V_{th} of 2 – 6 V for all the devices made with a-Si:H (1, 2) and SiN (1…4). The C–V characterization of our Al/c-Si/SiN/a-Si:H MIAS capacitors shows that the devices have a flat-band voltage, V_{fb} in the range of –2 up to –8 V for all the samples (see table 3.1).

a-Si:H sample	SiN sample	TFT sample	μ [cm^2/Vs]	V_{th} [V]	V_{fb} [V]
2	1	1	0.16	4.2	–8
1	2	2	0.24	5.5	–6.5
1	3	3	0.22	3.4	–3
2	4	4	0.17	2.5	–2

Table 3.1. Electrical parameters of as-deposited SiN films

The samples deposited at high plasma power exhibit a low mobility compared with sample deposited at low plasma power because of the rough interface that resulted between a-Si:H and SiN. A FTIR of the interface shows presence of SiH_2 bonds especially in TFT 2. Because SiH_2 bonds (peak number 2 in fig. 3.5) had been not detected in a-Si:H deposited on bare Si wafer, it means that the peak is due to plasma damage during deposition of a-Si:H. The origin of NH_2 bonds at the interface (peak number 3) is also related to plasma damage but in SiN.

The samples deposited with low N_2 flow exhibit a larger flat-band and threshold voltage compare with the samples deposited at high N_2 flow. Low N_2 flow also resulted in a SiN below stoichiometric; this film appears to have more positive fixed charge and/or more charge trapping sites than the stoichiometric film deposited at high N_2 flow. The result is a higher flat-band voltage in the below stoichiometric film than in the near-stoichiometric one.

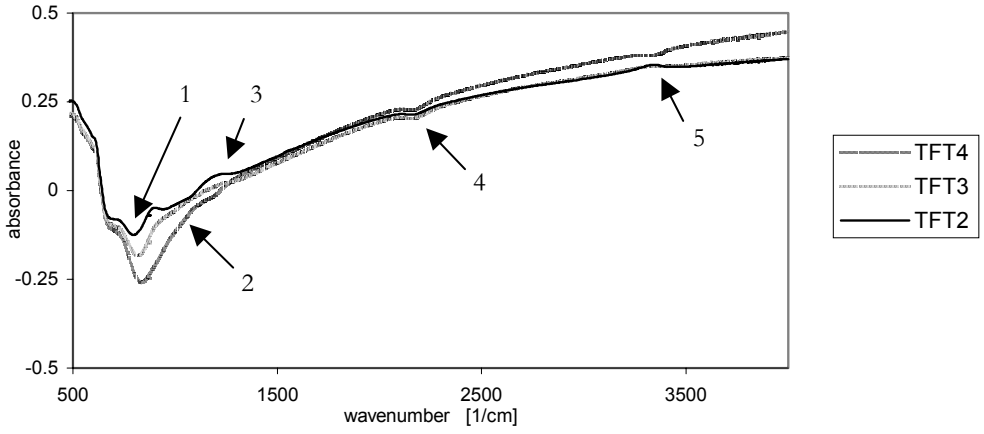

Fig. 3.5. FTIR spectra of the a-Si:H/SiN interface of four TFTs. The arrows indicate: 1 - Si-H wagging bonds in a-Si:H; 2 - Si-H_2 bonds in a-Si:H; 3 - N-H_2 bending in SiN; 4 - Si-H bonds in SiN; 5 - N-H bonds in SiN.

3.3. Device physics

The MOSFET operation and modelling of the current-voltage characteristics is extensively described in ref. [2] and [3].

Even though the equations that present the drain current function of gate voltage are the same for TFTs [4], the premises from which the deduction of the current equations are different. For example, the mobility, the field and charge distribution in the channel of a TFT are different comparing to MOSFET due to a high density of traps located in the a-Si:H band gap. As explained in chapter 2, the traps situated in the semiconductor band gap are tail and gap states that appear due to the disorder in the lattice plus deep gap or dangling bond states that appear due breaking of weak Si-Si bonds. The tail and gap states in a-Si:H gap (close to the edges of conduction and valence bands) are acceptor-like states located in the upper part of the gap and donor-like states located in the lower part of the gap. These states are modelled by an exponential energy distribution. The mid-gap or deep gap states are amphoteric dangling bond states explained in chapter 2. These states are modelled by a gaussian-like energy distribution.

Device modelling has been used to investigate the influence of a-Si:H deep gap states due to DBs on the TFT transfer characteristic. The model solves Poisson equation at room temperature in two cases where a-Si:H density of states, DOS is (1) dominated by tail states and gap states and DBs are reduced for example, by hydrogenation (2) DBs are not reduced; tail, gap and deep DBs states are all present in the gap. The density of free and trapped charge in a-Si:H, the density of free electrons at the surface, the band bending, the channel thickness and drain current as function of gate voltage are calculated with and without the band gap states due to DBs. The contribution of interface states to the total charge density is neglected.

The TFT is n-channel and in consequence, the contribution of holes under electron accumulation and the effect of drain and source resistances are neglected.

The model used in this section is based on the work of Shur, papers refereed in [5-8]. All model parameters are considered typical for a-Si:H and they are tabulated in the table 3.2. The model is written in Fortran programming language using an implicit routine. The surface band bending is swept on a linear grid from 0 to a maximum value of 0.8. For each point on this grid the Fermi

level is determined using the relation: $E_F = E_{F0} + \Psi$. The energy distribution of the total charge density is integrated on a linear grid over the band gap for the corresponding band bending. The surface induced charge is obtained by integrating the total charge density over the band bending from 0 to surface band bending. The gate voltage inducing this charge is calculated from $V_g = Q_{ind}/C_i + V_{fb}$, where the flat band voltage is taken zero. Each of all grids used consisted of 500 points.

$g_{ta} = 2 \cdot 10^{20}\ cm^{-3}eV^{-1}$	Density of the acceptor like tail states
$g_{da} = 5 \cdot 10^{18}\ cm^{-3}eV^{-1}$	Density of the acceptor like deep states
$E_{ta} = 0.021\ eV$	Characteristic energy for the acceptor like tail states
$E_{da} = 0.086\ eV$	Characteristic energy for the acceptor like deep states
$\mu = 13.8\ cm^{-3}eV^{-1}$	Band mobility
$E_c = 1.72\ eV$	Conduction band energy
$E_v = 0\ eV$	Valence band energy
$\varepsilon_s = 11 \cdot \varepsilon_0$	Semiconductor permitivity
$N_c = 2 \cdot 10^{20}\ cm^{-3}$	Conduction and valence band effective densities of states

Table 3.2. The a-Si:H parameters used in the calculation of trapped charge [5].

The acceptor-like tail and gap states are modelled by exponential distributions:

$$G_{ta}(E) = g_{ta} e^{\frac{E-E_c}{E_{ta}}} ; G_{da}(E) = g_{da} e^{\frac{E-E_c}{E_{da}}} \quad (1)$$

The density of trapped charge is calculated by integrating the product of the Fermi-Dirac occupation function and localized DOS.

$$n_t(E) = \int_{E_v}^{E_c} (G_{ta}(E) + G_{da}(E)) \cdot f(E) dE \quad (2)$$

where $f(E) = \frac{1}{1 + e^{\frac{E - E_F}{kT}}}$ is the equilibrium Fermi-Dirac occupation function with E_F the equilibrium Fermi level position.

The density of mobile carriers $n(E)$ is written as:

$$n(E) = N_c \cdot e^{\frac{-(E_c - E)}{k \cdot T}} \quad (3)$$

with N_c the effective density of states in the conduction band.

In the presence of DBs states, a term $n_{db}(E) = \int_{E_v}^{E_c} D(E) \cdot (f_n(E) - f_p(E)) dE$ is added to eq. 2; where $D(E)$ is the energy distribution of charged mid-gap defects and $f_n(E)$ and $f_p(E)$ are the occupancy functions for negative and positive charged defects, respectively (see appendix A). $D(E)$ is represented as a gaussian distribution of energy after ref. [9] (see appendix B). The occupancy functions are shown in appendix A and the calculation of $D(E)$ in appendix B.

The total density of free and trapped charge expressed in eq. 2 and eq. 3 as function of Fermi energy is shown in fig. 3.6.

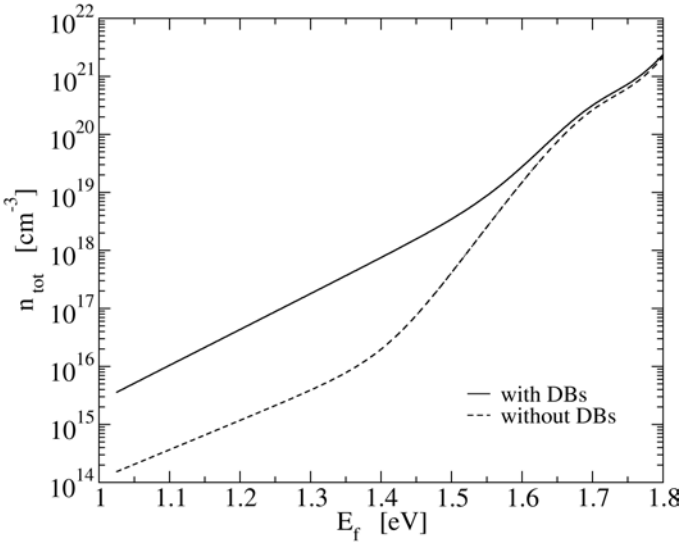

Fig. 3.6. Calculated total density of free and trapped charges in a-Si:H.

The electric field F (perpendicular to the channel with x space coordinate) distribution is found from the solution of the Poisson equation:

$$\frac{dF}{dx} = \frac{-q \cdot (n + n_t)}{\varepsilon_s} = \frac{\rho}{\varepsilon_s} \tag{4}$$

The Fermi level position and the band bending are related by: $E_F(x) = E_{F0} + \Psi(x)$ (see fig. 3.7) [10] where E_{F0} is the Fermi level in the bulk considered in the modelling as equal to $1.02\ eV$. This value corresponds to a Fermi level position above mid-gap due to the presence of a larger density of negatively charged defects in the lower gap of a-Si:H comparing to the positive defects and acceptor-like states in the upper gap. Using the relationship between the electric field and potential in the channel, Ψ that is $F = -\frac{d\Psi}{dx}$, the electric field function of band bending is written as:

$$F(\Psi) = \sqrt{\frac{2}{\varepsilon_s} \cdot \int_0^{\Psi} \rho(\Psi)\, d\Psi} \tag{5}$$

The computed dependence of the electric field on the band bending is shown in fig. 3.8.

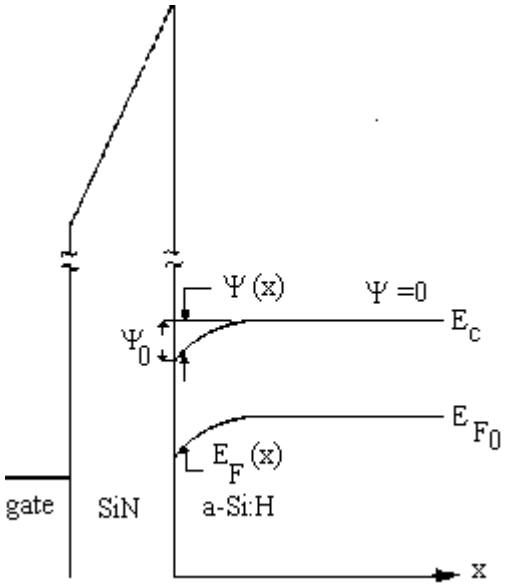

Fig. 3.7. Band diagram of an a-Si:H TFT [6] (the valence band is not shown)

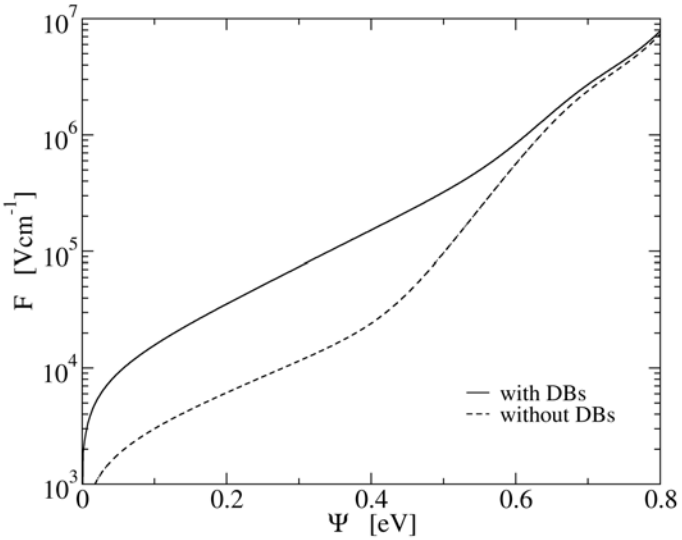

Fig. 3.8. Electric field as function of band bending

The total induced charge per unit area Q_{ind} and the free electron at surface per unit area $q \cdot n_s$ are given by:

$$Q_{ind} = \varepsilon_s \cdot F(0) = \sqrt{2 \cdot \varepsilon_s \cdot \int_0^{\Psi_0} \rho(\Psi)\, d\Psi} \tag{6}$$

$$q \cdot n_s = \int_0^{\Psi_0} \frac{n(\Psi) d\Psi}{F(\Psi)} \tag{7}$$

Where $F(x=0)=F(\Psi=\Psi_0)$ is the electric field at a-Si:H/SiN interface and Ψ_0 is the band bending at the interface. The values of $F(0)$ and Ψ_0 are found from an independent measurement of the charge induced in the channel (e.g. measurement of the drain current).

The potential distribution is found from the equation:

$$x = -\int_{\Psi_0}^{\Psi} \frac{d\Psi}{F(\Psi)} \tag{8}$$

Computed band bending function of distance from the interface for $V_g = 10$ V is presented in fig. 3.9.

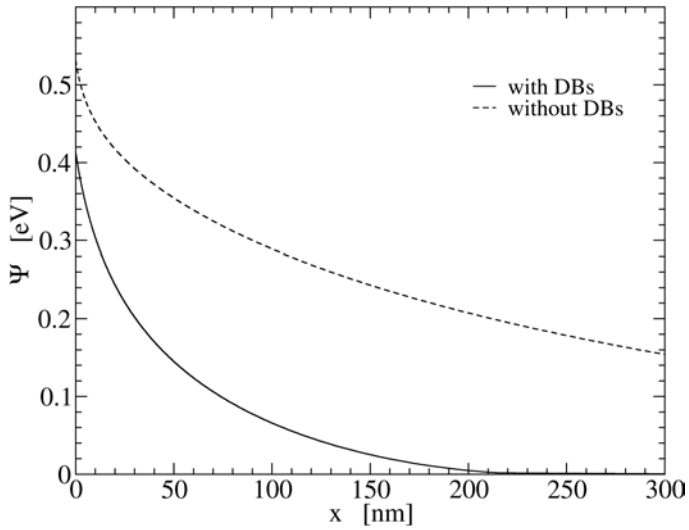

Fig. 3.9. Band bending function of distance for a gate voltage 10 V. a-Si:H layer thickness is 300 nm.

One notices that the band bending for the case when DBs are neglected is smaller than the band bending for the case when the DBs are taken into account. The relation $\frac{d\Psi}{dx}(x = d_{si}) = \Psi(d_{si}) = 0$ is not satisfied for the case without DBs (d_{si} is the thickness of the a-Si:H film), in this case Ψ decays to zero only to a distance equal to $500\ nm$ that is more than d_{si}.

The channel depth is calculated using the formula:

$$d_c = \frac{k \cdot T}{q \cdot F(0)} \tag{9}$$

The channel depth as function of band bending is shown in fig. 3.10.

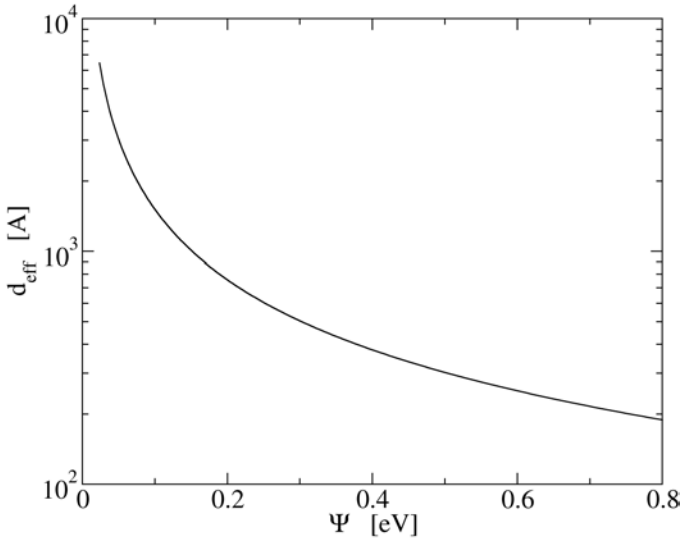

Fig. 3.10. The effective channel depth as function of band bending

The channel depth (eq. 8) does not change when DBs are added to the model. The explanation is that d_c depends inversely proportional to the surface field (fig. 3.8) and the difference between the surface field with and without DBs is very small; thus the channel depth is almost the same with/without DBs.

The relation between the gate voltage and the band bending is deduced via the equation $V_g = \frac{Q_{ind}}{C_i}$. In this equation the contribution of fixed charge has been neglected and C_i, insulator capacitance was calculated $17\ nF$. The band

bending for each applied voltage is shown in fig. 3.11. The surface density of free electrons from eq. 6 as function of gate voltage instead of Ψ is represented in fig. 3.12.

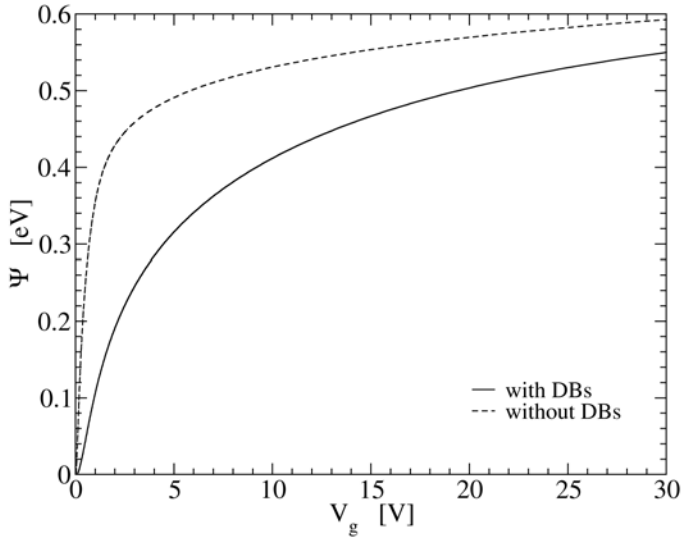

Fig. 3.11. Band bending as a function of the applied gate voltage.

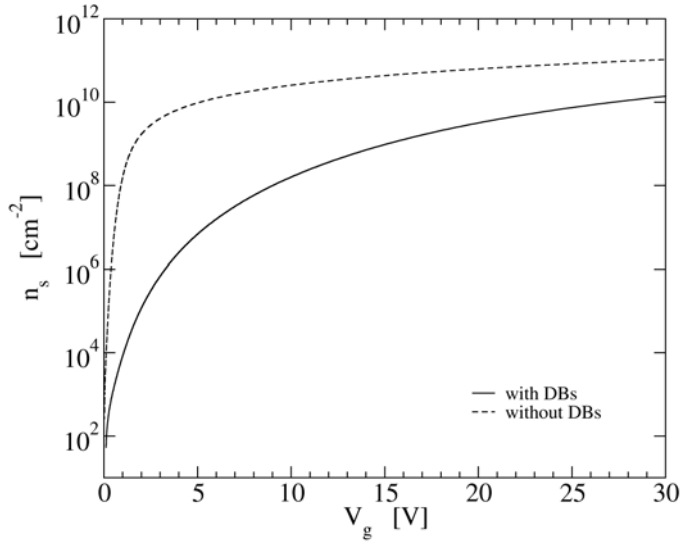

Fig. 3.12. Computed density of free electrons at surface (log scale) as a function of gate voltage

One notices that the surface density of free carriers is almost one order of magnitude smaller when DBs are taken into account than without DBs. That is

expected because there are more trapping sites in the a-Si:H gap for conductive carriers when DBs are taken into account.

The field effect mobility of a-Si:H is usually lower than $1\ cm^2V^{-1}s^{-1}$ whereas the electron band mobility is reported around $10\ cm^2V^{-1}s^{-1}$ [10]. The reason for the lower field effect mobility (μ_{eff}) relative to band mobility (μ) is the presence of shallow trap states that lead to a multiple-trapping conduction mechanism. Therefore, a large fraction of electrons resides in the trap states (tail states and gap and DBs states) and it is immobile. The above calculation of the charge trapped in tail and gap and DBs states is used to derive the field-effect mobility of electrons:

$$\mu_{eff}(E) = \mu \cdot \frac{q \cdot n_s(E)}{Q_{ind}} \tag{10}$$

Taking into account eq. 5 and 6, the ratio between field effect mobility and band mobility is represented in fig. 3.13 as a function of gate voltage.

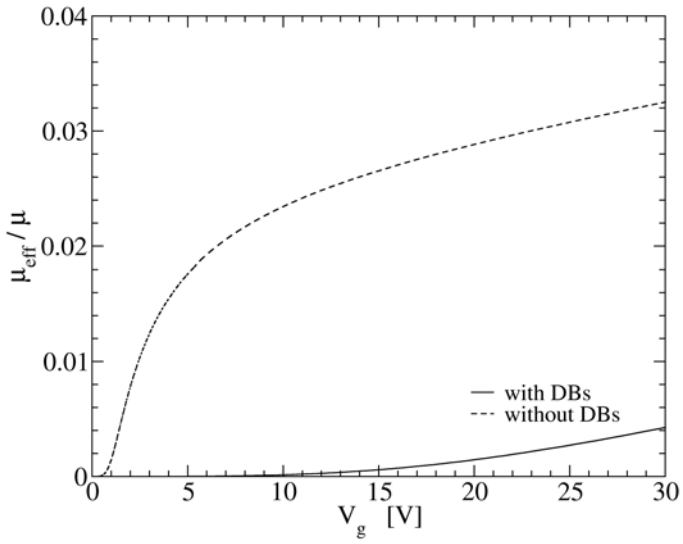

Fig. 3.13. Ratio of field effect mobility versus band mobility as a function of applied gate voltage.

The ratio $\mu eff/\mu$, also called relative mobility, is much smaller in the presence of DBs than without DBs; it can be noticed that an increase appears only at about $V_g = 10$ V and it does not increase substantially even at 30 V. This

is very different from the case of MOSFET where the mobility is almost independent on the gate voltage.

For a drain voltage $V_d << V_g$, the channel region acts like a resistor and the drain current can be expressed as:

$$I_d(V_g) = q \cdot \mu \cdot \frac{W}{L} \cdot \int_0^{V_d} n_S(\Psi) d\Psi \tag{11}$$

In fig. 3.14 the drain current as a function of applied voltage is shown at a small drain voltage $V_d = 0.5$ V and a W/L = 2.

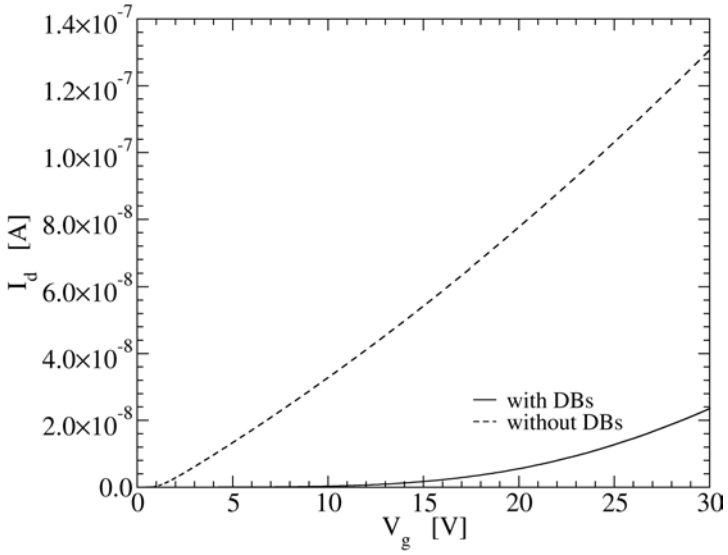

Fig. 3.14. Computed current function of gate voltage for $V_d = 0.5$ V

As it can be seen in fig. 3.14, the presence of DBs in a-Si:H band gap influences the I_d–V_g transfer characteristic and electrical parameters such as threshold voltage and subthreshold swing of a TFT. The drain current decreases about 1 order of magnitude comparing to the current computed in absence of DBs. If defining the threshold voltage as the gate voltage where the current has a value of 10^{-10} A, that threshold voltage is about two times smaller when the DBs are taken into account than when no DBs are present. It notices that the influence of DBs is significant in the subthreshold region because the curve computed without DBs is steeper than the curve where DBs are present. Thus the subthreshold swing is different with/without DBs.

3.4. Conclusion

The best device seems to be the device with films deposited at 60 W; plasma damage at 100 W results in a rough interface between a-Si:H and SiN. Because of that, the devices made with 100 W deposited films have a lower mobility comparing to the devices deposited at 60 W. High N_2 flow resulted in a insulator closer to stoichiometry and with a lower flat band voltage comparing to the nitride deposited at low N_2 flow.

Device modelling shows that the presence of DBs in the a-Si:H band gap strongly influences the TFT electrical parameters. In presence of DBs states, the mobility and drain current significantly decrease and the threshold voltage increases with respect to the case where no DBs are in the gap.

Appendix A

Occupancy functions for dangling bonds in thermodynamic equilibrium:

$$f^{+}(E)=\frac{1}{Z}$$

$$f^{0}(E)=\frac{2}{Z}\cdot\exp\left(-\frac{E-E_F}{k\cdot T}\right)$$

$$f^{-}(E)=\frac{1}{Z}\cdot\exp\left(-\frac{2\cdot E-2\cdot E_F+U}{k\cdot T}\right)$$

$$Z=1+2\cdot\exp\left(-\frac{E-E_F}{k\cdot T}\right)+\exp\left(-\frac{2\cdot E-2\cdot E_F+U}{k\cdot T}\right)$$

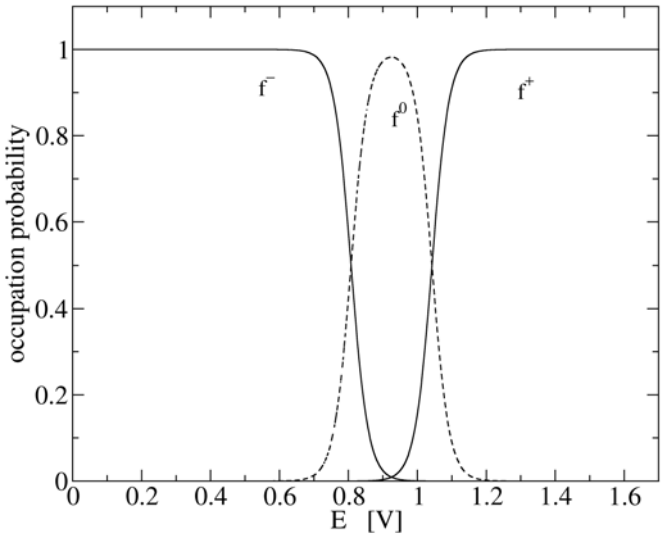

Fig. 3.A.

Where: f_p, f_i and f_n are the occupation functions for positive, neutral and negative DBs. U is the correlation energy U = 0.2 eV at T = 293 K.

The representation in fig. 3.A is made supposing a Fermi level at 1.02 eV.

Appendix B

The density of states at equilibrium are expressed in the relations below:

$$D(E) = \gamma \cdot \left[\frac{2}{f^0(E)} \right]^{\rho kT/E_{v0}} P\left(E + \frac{\rho\sigma^2}{E_{v0}} \right)$$

where the notation is:

$$\gamma = \left(\frac{N_{v0}E_{v0}}{1 - kT/2E_{v0}} \right)^{\rho} \left(\frac{i}{2 \cdot n_H} \right)^{\rho-1} \exp\left[\frac{-\rho}{2E_{v0}} \left(E_p - E_v - \frac{\rho\sigma^2}{2E_{v0}} \right) \right]$$

$$\rho = \frac{1}{1 - ikT/2E_{v0}}$$

P(E) is the energy distribution of sites that would form defects at energy E, so called defect pool function and it has the formula:

$$P(E) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left[\frac{-(E - E_p)^2}{2\sigma^2} \right]$$

The values of the constants used in modelling are listed in table 3.B.

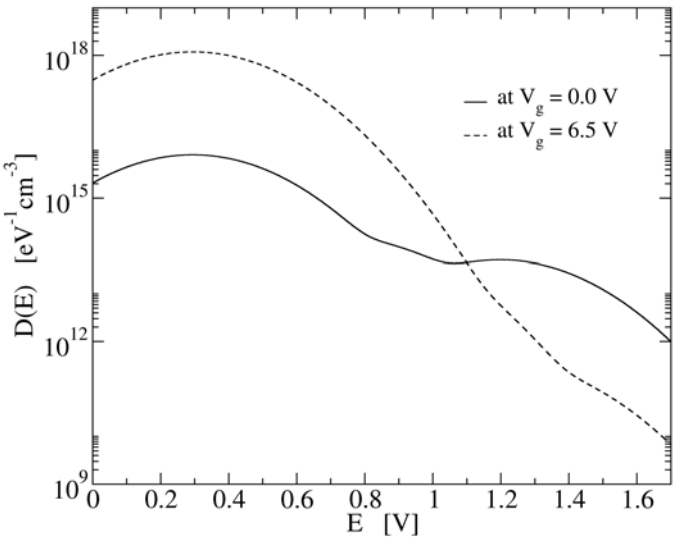

Fig. 3.B. The calculated density of DBs states at two gate voltages.

In fig. 3.B the negative defect is in the lower part of the gap and positive defect in the upper part of the gap; the neutral defect peak is not presented being not participant to the total induced charge. It can be seen that the peak of negative defects increases and the peak of positive defects decreases when increasing the gate voltage.

$N_{v0} = 2 \cdot 10^{21}\ cm^{-3}eV^{-1}$	Density of tail states at the valence band mobility edge
$E_{v0} = 0.045$ eV	Characteristic energy of the tail states at the mobility edge of valence band
$i = 2$	Number of H that are involved in involved in forming of Si-H pairs
$n_H = 5 \cdot 10^{21}\ cm^{-3}$	Volume density of hydrogen
$E_p = 1.2$ eV	The most probable energy in the distribution of available sites for defect formation
$\sigma = 0.178$	Width of defect pool

Table 3.B. Parameters used in the modelling of DBs states [9].

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CHAPTER 4

DEGRADATION MODELS

This chapter briefly presents the state-of-the art in the field of the a-Si:H metastability. The metastability of a-Si:H is in strong relationship with a-Si:H TFTs degradation. There are described the theoretical models in the literature regarding degradation of a-Si:H TFTs, focusing the attention on those characteristics that make the distinction between the models. Experimental threshold voltage shift obtained by stressing TFTs is fitted using the models described in this chapter.

4.1. Metastability of a-Si:H

This section summarises the knowledge of metastability in amorphous materials. The link between metastability of a-Si:H and the percentage of hydrogen in a-Si:H is made according to the literature in 4.1.1. The role of hydrogen in the metastability of a-Si:H is explained using the so called 'H-glass' model. The dispersive carrier transport in a-Si:H is briefly described in the light of a continuous time random walk and multiple trapping model in 4.1.2. In relation to dispersive transport, the time dependent H diffusion and carrier relaxation in amorphous materials is explained in 4.1.3.

4.1.1. Glassy nature of a-Si:H. The role of hydrogen.

The state of stable thermodynamic equilibrium is at a global minimum of free energy. But the metastable state is trapped in a local minimum of free energy.

Experimentally, metastability has been observed in glasses, chalcogenides, polymers and amorphous materials [1]. Regular glasses are amorphous solids created by a fast cooling (quench) of a liquid. Due to the slow kinetics, the molecules are 'frozen-in' and cannot reach their lowest-energy crystalline state. Well studied in the literature are the cases of irradiation-induced, field-induced

and thermally induced metastability [2]. However, usually systems can be driven out of metastability by strong enough perturbation (e.g. super-cooling of glass).

Glass is a solid, brittle material that has an amorphous, liquid-like structure without obvious fluidity. A glass forms when a typical liquid (a disordered molecular structure) is cooled to a temperature generally about $100\ °C$ below its equilibrium crystalline melting temperature or freezing point, at a rate sufficiently high to avoid crystallization of the liquid. This solidification process, known as vitrification, results in the 'freezing in' or immobilization of the disordered structure of the liquid state such that the resulting 'glassy' solid is spatially homogeneous, but without any long-range lattice order. The temperature (T_g) at which this transition occurs is called the glass transition temperature.

Above the glass transition temperature, the system is in a rubbery state (capable of flow in real time) and below T_g, the system is in a glassy state. The temperature T_g depends on experimental conditions, particularly logarithmically on the cooling rate. T_g depends as well on the type and amount of doping of the material.

Although it is a non-equilibrium structure, it is possible to anneal the glass, and encourage it to move towards equilibrium. Thus, a glass may 'densify' upon annealing, as it moves to a near equilibrium state that is another minimum of free energy.

Amorphous materials like a-Si also exhibit a glass transition upon cooling. The amorphous film equilibrates above T_g and the equilibrium is 'frozen in' when the film is cooled below T_g. At $T < T_g$, a-Si is in a metastable state, like glass [3]. If a sample is held at high temperature and then abruptly cooled down at room temperature, the structure will be 'frozen-in'. If the sample cools slowly to room temperature, the structure will be the equilibrium structure at room temperature.

T_g of a-Si is about $200\ °C$ for slow cooling rates ($1 - 100\ °C/min$); it is higher in undoped films and decreases with the doping.

It is widely believed that the metastability behaviour in hydrogenated amorphous materials is connected to the presence of hydrogen H [4]. The strongest argument comes from the quantitative agreement between the annealing kinetics of light-induced defects [5] and H diffusion [6].

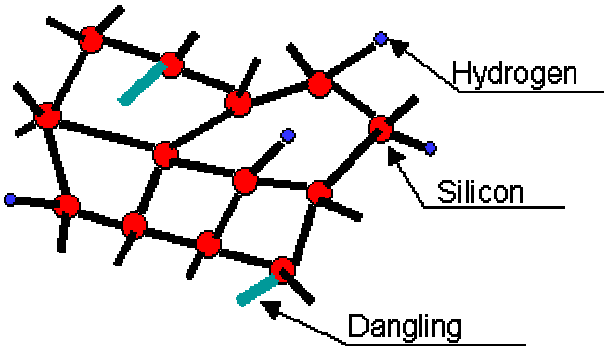

Fig. 4.1. A schematic picture of a-Si:H DBs, Si-Si bonds and Si-H bonds.

The amorphous nature of a-Si leads to a considerable density of localized states (tail states) and weak bonds with energy levels in the band gap of the material. Hydrogenation of a-Si introduces H as an additional structural component with high lattice mobility.

Such states are also called defects and play an essential role in a-Si:H films with respect to the metastability. Street and Jackson [7] improved the defect pool model, as discussed in chapter 2, proposing the breaking of Si-Si weak bonds and dangling bonds DBs formation due to H diffusion in the lattice as being the mechanism that would allow the Si network to rearrange. The a-Si:H network is represented in fig. 4.1.

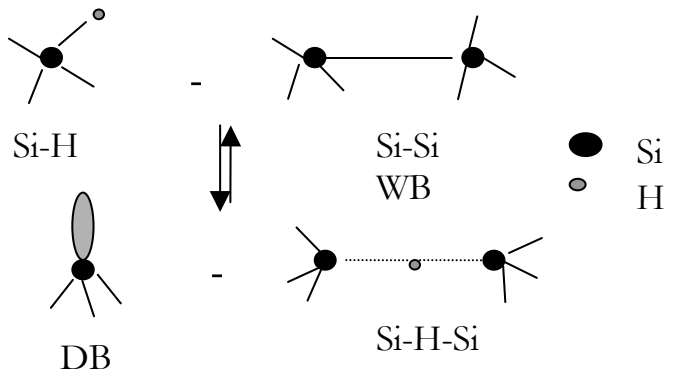

Fig. 4.2. Creation and passivation of DBs due to H motion.

The diffusion of H provides a mechanism by which DBs can be separated from intimate pairs into isolated DBs without changing the number of bonded sites. H in a-Si:H is either bonded in Si-H bonds or mobile in the interstitial sites. A possible reaction proposed for creation and passivation of dangling bonds is described in fig. 4.2. DB are created and passivated by short-range motion of H from Si-H bonds to weak Si-Si bonds. The defects are removed by annealing at $150 - 200$ °C. In this temperature range, significant diffusion of H occurs.

Based on the 'glassy' nature of a-Si:H and on the diffusion of H through the lattice, a so-called H-glass model [7, 8] was proposed to explain the metastability. According to the model, H atoms in a-Si lattice form a viscous fluid whose flow causes repeated bond breaking and re-formation when $T > T_g$. When $T < T_g$ the H is almost immobile. If a specimen is rapidly cooled from $T > T_g$ to $T < T_g$, the structural configuration before cooling is frozen in. At $T < T_g$ this specimen would show a slow relaxation towards the structure it would have attained over a slow cooling process.

The time dependence of the rate of defect formation and removal are intermediated by H diffusion and they were explained by the following kinetic equation [9]:

$$\frac{dN_{db}}{dt} = D_h(t) \cdot (A \cdot n_{bt} - B \cdot N_{db}) \qquad (1)$$

where N_{db} is the DB density and n_{bt} is band-tail carriers density; A and B are constants expressing the hydrogen density multiplied with capture radius; D_h is the time dependent hydrogen diffusion coefficient. In eq. 1, the first term represents the formation of defects proportional to the band tail carrier density and H diffusion coefficient and the second term represent the defects annealing (or passivation) proportional to the defect density and, again H diffusion coefficient.

However, H is not a prerequisite for DBs formation. Crandall proposed alternatively a model without involving the hydrogen motion [10].

An experiment in determining whether H diffusion in a-Si:H lattice is the only responsible mechanism for a-Si:H metastability requires variations of the H percentage or bonding configuration. The variation of the deposition conditions

that this kind of experiment would impose, affects also the optical band gap, extent of the band tails and other electronic properties of the material. Thus, it is difficult to prove that the metastability issues in a-Si:H are the exclusive result of H diffusion. Time-dependent H diffusion, so called 'anomalous' H diffusion, is briefly explained in section 4.1.2.

4.1.2. Anomalous hydrogen diffusion

It is found by experiments of Butcher [11] that, in an amorphous semiconductor, a sheet of charge injected at one side of the sample does not travel to the other side as a single packet with a well-defined velocity but it suffers a considerable degree of dispersion. If the density of states is constant, a packet in energy space evolves into Gaussian one, moving with constant velocity and mean square deviation increasing linearly in time. But, if the density of states decreases exponentially with decreasing energy, the motion of the packet tremendously slows down with time.

As an immediate consequence of dispersion is the 'anomalous' time dependent H diffusion, which origins are largely described in ref. [9, 12-16]. The equation that describes hydrogen diffusion through the amorphous lattices, so-called diffusion-dispersive equation is $D_h = D_0 \cdot t^{-\alpha}$, where D_0 is a pre-diffusion proportionality constant and α is temperature dependent dispersion parameter. In ref. 12 and 13 the hydrogen diffusion is explained as based on continuous time random walk (CTRW) theory. According to this model, anomalous diffusion appears because of random walk and random pausing time of H atoms between localized states.

Because CTRW theory will be later on (in 4.2.1) refereed in relation with a charge-trapping model, some words are meant to briefly explain its content.

The idea of the model is that carriers do not have a 'normal' walk as defined by a Brownian motion for example, but jump between localized states with random lengths of jumps and pause a certain time at each stop (fig. 4.3). In glassy materials, this randomness in the carrier motion appears because of disorder in atomic network and thus high density deep traps that results from bonds irregularities.

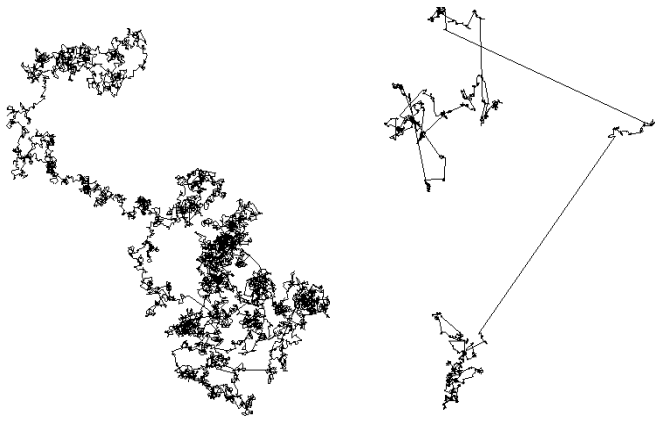

Fig. 4.3. Normal walk on left and CTRW on right
(http://chaos.ph.utexas.edu/research/annulus/rwalk.html)

In the context of carrier transport, it is more important how much time a carrier spends between jumps than the length of the jump itself. This dispersive transport can in general be represented by a probability density function of waiting times, $\Psi(t)$, which describes each particle jump in time t. For large pausing time, the density function obeys a power law decay as $\Psi(t) \approx t^{-1-\alpha}$, with an exponent $0 < \alpha < 1$ [14], $\alpha = 0$ tends to normal diffusion while $\alpha = 1$ tends to ballistic transport. After mathematical considerations expressed in ref. [9] and [15], the calculation of H diffusion coefficient is expressed as a power decay $t^{-\alpha}$.

Slow relaxation in glassy materials has been demonstrated as well in the context of CTRW [15]. In section 4.1.3 a more direct way to derive the relaxation equation is presented as starting from the diffusion equation.

Tiedje [16] shows that CTRW and multiple trapping of the carriers in the localized states of the conduction band tail are equivalent and can account for transport properties of a-Si:H invoking an exponential approximation like e^{-E/kT_0} for the band tail density of states, where k is the Boltzmann constant and kT_0 is the characteristic energy of the exponential distribution of the trapping sites with T_0 in the range of $200 - 290$ K.

According to Jackson [17], the anomalous diffusion appears because of H trapping in an exponential distribution of defects in the band tail of a-Si:H. Schirmacher show that dispersive transport and relaxation of the carriers from

traps are intimately connected by H diffusion [18, 19]. Relaxation of carriers is described by the stretched exponential equation that is derived in section 4.1.3.

4.1.3. Stretched exponential relaxation

The relaxation of electronic and molecular systems was first studied by Kohlrausch in 1846 [20]. He found that the time decay of the residual charge on a Leyden glass jar was described by a function $\exp\left(-(t/\tau)^{\alpha}\right)$ called stretched exponential function. The work of Kohlrausch was continued by Williams and Watts [21] and evolved into a universal law that characterized the disordered systems. An extensive overview upon the work dedicated to stretched exponential relaxation in molecular and electronic glass is given in ref. [22].

In this section, the relaxation of carriers to DBs is studied and the stretched exponential equation is derived starting from the assumption that H is the precursor of defect creation and that H has a time-dependent diffusion constant.

In annealing experiments, the devices allow to relax at 0 V. In this case, the negative charged defects lose their electrons and become neutral. The DBs number becomes larger than the band-tail carriers number and the first term of eq. 1 can be neglected [17].

Eq. 1 becomes a differential equation $\frac{dN_{db}}{dt} = -B \cdot D_h \cdot N_{db}$, where $D_h(t) = D_0 \cdot (t)^{-\alpha}$ with $0 < \alpha < 1$ and $D_0 = D_{00} \cdot \nu^{-\alpha}$, where D_{00} is a proportionality constant and ν is H attempt-to-escape frequency. The solution of this equation gives the time dependence of the DBs density during relaxation in the form of a stretched exponential decay:

$$N_{db}(t) = N_0 \cdot \left(\exp\left(-\left(\frac{t}{\tau} \right)^{1-\alpha} \right) \right) \qquad (2)$$

where $N_0 = N_{db}(0)$ is the initial density and is constant; $\tau^{\alpha-1} = \frac{D_0 \cdot B}{1-\alpha}$ and $1-\alpha = \frac{T}{T_0}$ where kT_0 is the characteristic energy of traps, and T_0 is a characteristic temperature, typically in the range of $500 - 600$ K. Parameter τ is usually known in the form $\tau = \tau_0 \cdot \exp\frac{E_a}{kT}$ where $\tau_0 = \frac{1}{\nu}$ and $E_a = kT_0 \cdot \ln\left(\frac{1-\alpha}{B \cdot \tau_0 \cdot D_{00}}\right)$ is trap activation energy. This form results after mathematical re-calculation from the formula $\tau^{\alpha-1} = \frac{D_0 \cdot B}{1-\alpha}$ and it shows τ like a trap-release characteristic time; those traps are exponentially distributed with activation energy E_a and the distribution slope kT_0. Values such as E_a = 1.26 eV, $\tau_0 = 2 \cdot 10^{-13}$ s and T_0 = 500 K have been reported to fit experimental data [17].

4.2. Models for device instability

It is already known that the electrical characteristics of a-Si:H/a-SiN:H interfaces are altered by both dielectric and semiconductor interface traps [23]. Many papers present different methods to distinguish the contribution of semiconductor traps and insulator traps. The most common approach in studying the a-Si:H/SiN TFTs degradation is the time dependence of the threshold voltage when the device is subjected to stress. Two classes of models for threshold voltage degradation evolved as models attributing the threshold voltage shift to charge trapping in the gate insulator and models attributing the shift to defect creation in the semiconductor.

In the next sub-sections 4.2.1 and 4.2.2, two models from each class are presented. These models are the newest trend in studying a-Si:H TFTs degradation of the threshold voltage during gate voltage stress. Which one describes in a better way device degradation is subject of a long debate in the scientific community due to different mechanisms they propose to account for. The models are many times referenced throughout this thesis and the equations

they propose fit experimental data; therefore, the fundamental equations that result from the models are derived in the following sections.

4.2.1. Charge trapping. Dispersive injection model.

Charge trapping in SiN was initially proposed in the work on MNOS memory devices [24]. The models of charge trapping in the insulator are divided in two main groups based on: the tunnelling of electrons from the silicon conduction band to unoccupied traps below the Fermi level in the insulator for low to medium insulator field [25] and Fowler-Nordheim tunnelling at high field in the insulator [26]. In practice, in TFTs, the gate insulator field is low (< 1 MV/cm) therefore only the charge trapping in the gate insulator at low electric fields is to be discussed.

The first publications on the a-Si:H/SiN TFT instabilities reported a threshold voltage shift having a logarithmic time dependence $\Delta V_{th} = V_0 \cdot \ln\left(1+\frac{t}{t_0}\right)$ [27]; where $V_0 = V_g - V_{th}(0)$ and $t_0 = \nu^{-1} \cdot \exp(E_a/kT)$ with $V_{th}(0)$ - the initial threshold voltage, V_g - gate voltage, ν - attempt to escape frequency and E_a - activation energy, k - Boltzmann constant and T - temperature. The shift was attributed to charge trapping in SiN. Measurements performed later on ambipolar devices show that, at low and moderate gate voltage shift, the defect creation in a-Si:H dominates the threshold voltage shift whereas at high electric field or low quality SiN, the charge trapping dominates [28, 29].

It has been shown by many authors that the charge trapping cannot be neglected completely when studying the TFT degradation and that the trapping is rather a rate-limited mechanism that occurs at the interface than in the insulator bulk [30]. The dispersive injection model [31, 32] describes the threshold voltage shift time-dependence as an effect of the charge trapping/detrapping at the interface between semiconductor and insulator. It was successfully applied to explain the threshold voltage shift in electrically stressed a-Si:H/a-SiO_x:H TFT.

According to this model, during gate stress, the charge from the accumulated active layer enters the gate insulator and is trapped into empty states of a highly defective region (transitional region) of the insulator, close to the

interface with the semiconductor. The charge transport occurs via hopping through localized states as described in CTRW theory presented in 4.1.2.

The time dependent injection of electrons from a-Si:H gap states into the insulator transitional region is described by an equation that resembles the rate of electron capture described in Schockley-Read-Hall statistics [33]:

$$\frac{dN_a(t)}{dt} = -N_a(t)\cdot(N_i - n_i(t))\cdot k(t) \tag{3}$$

where N_a is the charge/cm^2 in amorphous semiconductor; N_i is the number/cm^2 of available traps in the transitional region of the insulator; n_i is the number/cm^2 of filled traps in transitional region; $k(t)$ is a time dependent cm^2/s term written as a diameter $2\cdot r$ (r-trap capture radius) swept out by an electron hopping with a dispersive velocity v_d per unit time. For a power law distribution of hopping (or pausing) time it has been shown in CTRW theory that velocity holds as $v_d \propto \frac{N_a(t)}{\varepsilon_s}\cdot t^{\alpha-1}$ [34], where $N_a(t)/\varepsilon_s$ represents the electric field perpendicular to the surface; ε_s is the semiconductor permittivity and α is the dispersion coefficient. Thus, $k(t) = \frac{N_a(t)}{\varepsilon_s}\cdot t^{\alpha-1}\cdot 2\cdot r\cdot C$; where $\alpha = T/T_0$ and kT_0 corresponds to the characteristic energy of the traps; C is a proportionality constant. Reported T_0 is in the range $200 - 290$ K.

For small $n_i(t)$, the differential equation 3 is re-written as:

$$\frac{dN_a(t)}{dt} = -N_a^2(t)\cdot N_i\cdot t^{\alpha-1}\cdot B \tag{4}$$

where B is a proportionality constant that is equal to $2\cdot r\cdot C/\varepsilon_s$.

In this section, the time dependence of the threshold voltage shift is derived based on the theory available in ref. [3, 31, 32].

Assuming charge conservation:

$$N_a(t) + n_i(t) = C_i \cdot V_g^* \tag{5}$$

where C_i is the insulator geometrical capacitance, $V_g^* = V_g - V_{fb}$ and V_g is the stress gate voltage and V_{fb} is the flat-band voltage before stress is applied. The number of filled traps is given by $n_i(t) = C_i \cdot \Delta V_{th}(t)$

Solving eq. 4 with the initial condition $N_a(0) = C_i \cdot V_g^*$, the threshold voltage shift has the form:

$$\Delta V_{th}(t) = V_g^* \cdot \left(1 - \frac{1}{1 + \left(\frac{t}{\tau} \right)^{\alpha}} \right) \tag{6}$$

with $\tau^{\alpha} = \dfrac{\alpha}{B \cdot C_i \cdot N_i \cdot V_g^*}$

This formula of the time-dependence of threshold voltage shift links directly the shift to the flat-band voltage, which it is related to the changes in the charge in the insulator.

4.2.2. Carrier-induced defect creation. Defect creation model.

In this sub-section, the defect creation model is discussed and the expression of the threshold voltage shift is derived accordingly.

The defect creation is based on the defect pool model [35-38]. Powell and Deane originally interpreted the creation/removal of dangling bonds with defect pool model [39, 40]. According to this, the creation and removal of states depends on the position of the Fermi level with respect to the conduction band. When the gate bias is swept from electron accumulation to hole accumulation, the Fermi level is swept through the band gap. The difference between the

electron ΔV_{th}^{e} and hole ΔV_{th}^{h} threshold voltage shift, measurable in ambipolar devices, is proportional to the change in the number of electronic states that change their charge state according to the change in the Fermi level position. If the states are assumed to be created in pairs (amphoteric DBs), then the change number of DBs (N_{db}) relates to the total change in threshold voltage as:

$$\Delta N_{db} = \frac{C_i \cdot \left(\Delta V_{th}^{e} - \Delta V_{th}^{h}\right)}{2 \cdot q} \tag{7}$$

The change of insulator charge is considered to be:

$$\Delta Q_i = C_i \cdot \left(\Delta V_{th}^{e} + \Delta V_{th}^{h}\right) \tag{8}$$

During stress, an equal number of D^- and D^+ defects shall be created therefore, $\Delta V_{th}^{e} = -\Delta V_{th}^{h}$ with $\Delta V_{th}^{e} > 0$ and $\Delta V_{th}^{h} < 0$.

Since the shifts are equal, it follows that a shift in the quantities in eq. 7 and 8 are written as: $\Delta N_{db} = \frac{C_i \cdot \Delta V_{th}}{q}$. These equations show that, in the light of this model, ΔV_{th} increases as the density created DBs in a-Si:H increases and any influence from the insulator is neglected.

Deane stated that in a device with spatially inhomogeneous density of states as a-Si:H, the concept of flat band voltage is meaningless [39]. V_{fb} should be regarded as 'apparent' flat-band voltage i.e. it should represent the gate bias for which the band bending induced by defects is counterbalanced. In this respect, the threshold voltage shift is due to the changes in interface and bulk semiconductor states. This consideration distinct the defect creation model from the dispersive injection model where the threshold shift is correlated to the changes in flat-band voltage.

The time dependence of the threshold voltage shift will be derived in the following.

When the device is subjected to electrical stress, e.g. gate voltage stress, the defects will be generated with a rate described by eq. 1. It is shown by Jackson that the creation rate is faster than the annealing rate at room temperature, therefore A >> B and the second term of the equation can be neglected.

Now, the defect creation rate is described by the differential equation: $\frac{dN_{db}}{dt} = A \cdot D_h \cdot (n_{bt})$; where n_{bt} is the density of band-tail states and D_h is H diffusion coefficient. Considering that DBs are the only defects in a-Si:H, the charge neutrality in intrinsic a-Si:H yields: $n_{bt} = -N_{db}$ and the solution of the differential equation yields $n_{bt}(t) = n_{bt}(0) \cdot \left(\exp\left(-\left(\frac{t}{\tau} \right)^{1-\alpha} \right) \right)$.

For a gate voltage V_g, the change in the density of band tail states is written as:

$$\Delta n_{bt} = C_i \cdot (V_g - \Delta V_{th}(t)) = -\Delta N_{db} \tag{9}$$

Replacing n_{bt} from eq. 9 in the solution of the differential equation of defect creation rate and taking into account the neutrality condition, a commonly used formula of the stretched-exponential equation appears:

$$\Delta V_{th}(t) = V_0 \cdot \left(1 - \exp\left(-\left(\frac{t}{\tau} \right)^{1-\alpha} \right) \right) \tag{10}$$

where $V_0 = V_g - V_{th}(0)$; V_g is the gate voltage and $V_{th}(0)$ is the initial threshold voltage. Again, like in section 4.1.3, parameter τ can be written in the form $\tau = \tau_0 \cdot \exp\frac{E_a}{kT}$ where $\tau_0 = \frac{1}{\nu}$ and $E_a = kT_0 \cdot \ln\left(\frac{1-\alpha}{A \cdot \tau_0 \cdot D_{00}} \right)$ is the trap activation energy. Values such as $E_a = 0.98\ \text{eV}$, $\tau_0 = 6 \cdot 10^{-10}\text{s}$ and $T_0 = 600\ \text{K}$ have been reported to fit experimental data [17].

For short times, eq. 10 becomes $\Delta V_{th}(t) = V_0 \cdot \left(\frac{t}{\tau}\right)^{1-\alpha}$.

Since the stretched exponential equation is intensively used in discussion about V_{th} degradation, it is necessary to mention that different authors found very different values for the characteristic time. Values of 10^6 s for characteristic time are usually related to defect creation/removal and values of $10^8 - 10^{11}$ s are related to charge trapping in the gate insulator [41, 42]. Reported α ranges from 0.2 to 0.6 and does not show any correlation between these values and the presumed mechanism for degradation.

Wehrspohn, Deane and Powell [43, 44] argument that the defect creation rate equation (eq. 1) underestimates the contribution of band tail carriers to the formation rate of DBs. Their argumentation is based on research of many authors who report a dispersion coefficient $\alpha_0 - \alpha = \frac{T}{T_0}$ rather than $1 - \alpha = \frac{T}{T_0}$.

Recalling the work of Schirmaker [45], Jackson showed that the coefficient of H diffusion depends also on the density of band-tail carriers as $D_h = D_{00} \cdot \nu^{-\alpha} \cdot t^{-\alpha} \cdot \left(\frac{n_{bt}}{N_c}\right)^{\beta}$ where N_c is the effective density of states in the conduction band. Based on this, Wehrspohn, Deane and Powell derived a new defect creation rate equation.

The new equation holds as: $\frac{dN_{db}}{dt} \propto D_h \cdot (n_{bt})^{\beta}$ with $2 > \beta > 1$. Solving this differential equation, an improved, semi-empirical equation to describe defect creation under electron accumulation emerged as: $n_{bt}(t) = n_{bt}(0) \cdot \left(1 - \frac{1}{\left(1 + \left(\frac{t}{\tau}\right)^{\alpha}\right)^{1/\varepsilon}}\right)$; where $\varepsilon = \beta - 1$ and $n_{bt}(0)$ is the initial density of band tail carriers.

The threshold voltage shift is obtained from this equation taking into account eq. 9:

$$\Delta V_{th}(t) = V_0 \cdot \left(1 - \frac{1}{\left(1 + \left(\frac{t}{\tau} \right)^{\alpha} \right)^{1/\varepsilon}} \right) \tag{11}$$

A reasonably good fit of experimental data is reported in ref. [43] for $1/\varepsilon = 2$ and this value will be used in this thesis wherever this model is mentioned.

For their improved carrier-induced defect creation model, the authors simplified eq. (11) by introducing the thermalization energy concept. The simplified concept of defect creation assumes that the defects are created via an exponential distribution of barriers that can be either a distribution of weak bonds, or a distribution of barrier heights or a combination of both. This improved defect creation model does not present a specific microscopic mechanism of defect creation. The thermalization energy is defined as $E_{th} = k \cdot T \cdot \ln(\nu \cdot t)$ [46]; where ν is attempt to escape frequency, reported as 10^{10} Hz. It is assumed that after a time t at temperature T all potential defect sites with energy barrier $E \le k \cdot T \cdot \ln(\nu \cdot t)$ are converted into defects. It is defined as well the activation energy of defect formation as: $E_a = k \cdot T_0 \cdot \ln(\nu \cdot t)$ where kT_0 is considered the slope of the exponential distribution of barrier states. Substitution of t from this equation into eq. 11 yields the threshold voltage shift written as a function of E as:

$$\Delta V_{th}(t) = V_0 \cdot \left(1 - \frac{1}{\left(1 + e^{\frac{E_{th} - E_a}{k \cdot T_0}} \right)^2} \right) \tag{12}$$

One notices that eq. 11 and eq. 6 show a similar $\left(1-\frac{1}{\left(1+\left(\frac{t}{\tau}\right)^{\alpha}\right)^{1/\varepsilon}}\right)$ time-dependence of the threshold. The factor in front of this time function is dependent on the initial condition of the device. In eq. 11 it is dependent on the initial threshold voltage and in eq. 6 is on the initial flat band. The initial threshold depends on the flat band before stressing, therefore, the similarities are even more striking. It can be said that starting from different premises, the equations deduced in the models are not very different and themselves cannot make a difference in fitting without the comparison of the fitting parameters α and τ.

In the next section, the threshold voltage shift time-dependence equations that result from de models described in section 4.2 are used in fitting the experimental data obtained after long-time stressing at room temperature of a commercial TFT.

4.3. Threshold voltage degradation

This section shows the results of fitting experimental data with the two models presented in 4.2.1 and 4.2.2. The threshold voltage shift obtained after long time gate voltage stressing two commercial TFTs (on the same glass) at room temperature has been fitted with dispersive charge trapping equation (eq. 6), with stretched exponential equation of the defect creation model (eq. 10) and with stretched hyperbola (eq. 11) of the improved defect creation model.

Two TFTs are subjected to different stress time at the same gate voltage stress. For the test, fresh annealed devices have been used. The TFTs have been subjected to 35 V gate stress for a total stress time 10^3 and 10^4 s. At a certain period, the stress was interrupted and the threshold voltage has been extracted from the transfer characteristics. The time between two measurements of the threshold voltage was short (5 min) for the device subjected to short stress time

(TFT1) and longer (30 min) for the device subjected to longer stress time (TFT2).

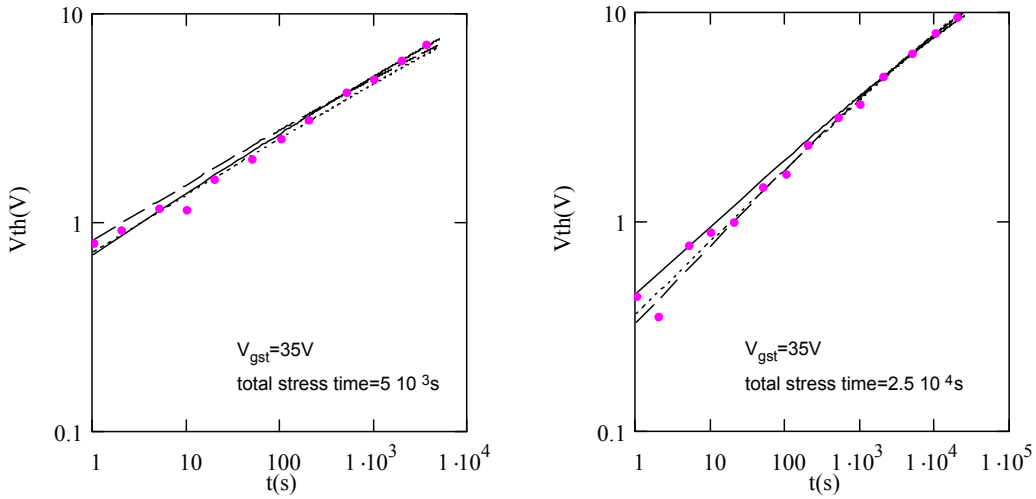

Fig. 4.4. Threshold voltage versus stress time (log-log plot). Experimental data were fitted with stretched hyperbola (solid), stretched exponential (dotted) and dispersive equations (dashed). TFT1 to the left, TFT2 to the right.

The threshold voltage shift was fitted with the stretched exponential, stretched hyperbola and dispersive equation that have been presented in sections 4.2.1 and 4.2.2 (fig. 4.4). The parameters of fitting are shown in an appendix to this chapter. The result of fitting shows that all models of dispersive charge trapping and defect creation are in good agreement with the experimental data. But even at long stress time (TFT2) it did not appear as significant that one of the mechanisms prevail upon the other.

The dispersion coefficient α has close value 0.28 – 0.3 (TFT1) and 0.38 – 0.33 (TFT2) for all three fits presented above. The characteristic time of the traps, τ was different in each model and for each TFT. On one hand, a different τ is expected since each model takes into account the trapping in different traps at the interface, in a-Si:H or in SiN. On the other hand, a similar α value for TFT1 and 2 calculated using the three equations mentioned above suggests that α is a parameter characteristic to H diffusion irrespective to the mechanism of diffusion (creation of DBs, hopping).

According to the results of the fitting for both TFT1 and 2 using the stretched hyperbola equation, the degradation at room temperature is caused by

changes in the interface charge density and not in the semiconductor bulk (similar values of α and τ for TFT1 and 2).

4.4. Conclusion

Both models of charge trapping and defect creation describe the time dependence of the threshold voltage shift. An experiment of long-time stressing TFTs at room temperature did not show a distinction between the models. It means that, for experiments at room temperature at least, it cannot be generalized that just one degradation mechanism is presented in all a-Si:H/SiN devices. Fitting of experimental data with one model does not show without any doubt that the degradation is due to one mechanism.

In chapter 5 it will be demonstrated that the bias induced degradation in a-Si:H/SiN TFTs at room temperature involves not only changes in the threshold voltage but also in the flat-band voltage and subthreshold swing.

Appendix

Parameters of the models used for fitting in fig. 4.3.

Legend:

TFT1 - the device subjected to a short period of stress

TFT2 - the device subjected to a longer period of stress

DCI - Dispersive charge injection

SE - Stretched exponential

SH - Stretched hyperbola

MODEL	PARAMETERS TFT1	PARAMETERS TFT2
DCI	$V_g^* = 33.5$ V $\tau = 6 \cdot 10^7$ s $\alpha = 0.28$	$V_g^* = 31.3$ V $\tau = 2 \cdot 10^5$ s $\alpha = 0.38$
SE	$V_0 = 33.4$ V $\tau = 10^6$ s $\alpha = 0.28$	$V_0 = 31.2$ V $\tau = 3.5 \cdot 10^5$ s $\alpha = 0.35$
SH♠	$V_0 = 33.4$ V $\tau = 4 \cdot 10^6$ s $\alpha = 0.3$	$V_0 = 31.2$ V $\tau = 3.3 \cdot 10^6$ s $\alpha = 0.33$

♠ The corresponding values calculated with eq. 12 are $E_a \sim 0.9$ eV and $kT_0 \sim 0.08$ eV

References chapter 4

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CHAPTER 5

BIAS STRESS DEGRADATION

In this chapter, the threshold voltage, subthreshold swing and flat band voltage have been determined from I–V and C–V measurements as function of stress time for different gate bias stress. Afterwards the subthreshold swing and the flatband voltage have been correlated with the threshold voltage.

5.1. Introduction

Two widely accepted mechanisms for threshold voltage shift in a-Si:H TFTs are defect creation and charge trapping. The mechanisms are described in chapter 4, sections 4.2.1 and 4.2.2. The time dependence of the threshold voltage shift as derived from each of the two models is presented as well in chapter 4.

It is reported in the literature that the defect creation in a-Si:H channel and bulk occurs at positive gate stresses lower than critical voltage while charge trapping in SiN occurs at positive gate stresses higher than critical and at negative gate stresses [1]. In the devices with poor insulator or Si-rich SiN, the charge trapping may appear at gate voltages smaller than critical [2]. Different magnitude ranging from 45 V to 55 V has been reported for critical gate voltage in TFTs [3]. In the bias stress measurements presented here, the stressing bias was set at lower voltage (10 and 35 V) than critical in order to eliminate the possible influence of the charge trapping in the bulk of the insulator.

In the literature, the defect creation rate is dependent on the temperature, whatever process causes the defects: stressed bond breaking and/or H diffusion. At elevated temperatures (above 200 °C) the DBs and the pool of potential DBs are in equilibrium [4] determined by the position of the Fermi level. As cooled through the equilibration temperature, the defect distribution is frozen into lattice and changes on large time scales. At room temperature, for example, the DBs distribution is considered frozen into lattice, new DBs can be created by electrical stress or illumination stress but the removal of DBs is insignificant [5].

The Fermi level position can be altered by gate stressing of the device causing a change in the defect charge state but not on the defect density. However, the Fermi level is not only shifted at the surface of a-Si:H but, to a lesser extent, to the a-Si:H bulk thus leading to a spatial inhomogeneity of DBs. If the gate bias is applied during an annealing cycle (200 – 220 °C), process called bias annealing, the density of states changes significantly and in short time [6].

But there is research showing that the defect creation and removal appear as well in bias stress measurements at room temperature [7, 8, 9], without thermal bias annealing.

The charge trapping is considered to be less sensitive to temperature [10]. But there are also papers explaining the temperature dependence of the threshold degradation in the light of charge trapping [11].

With so many interpretations of the temperature dependence of threshold degradation, a lot of research focuses on bias stress measurements at room temperature. The reason for this is that in normal operating conditions, a TFT withstands prolonged bias stress at room temperature. In the work presented in this chapter, the bias stress measurements had been performed at room temperature if not stated otherwise. The work presented in this chapter studies the changes induced by gate voltage stress in the threshold voltage, subthreshold swing and flat-band voltage.

5.2. Bias stressing the a-Si:H/SiN TFTs

5.2.1. Devices under test

The DUTs (device under test) were Al/ n type c-Si/ SiN/ a-Si: H/ Al TFTs with slightly sub-stoichiometric SiN (Si-rich) corresponding to TFTs 4 described in table 3.1 and Metal – Insulator – Amorphous Silicon - Silicon (MIAS) capacitors deposited on the same wafer. The devices have been annealed 0.5 hour in vacuum at 250 °C and cooled down to room temperature.

Other devices used are ambipolar a-Si:H/SiN TFTs with N-rich SiN and MIAS capacitors on the same plate as described in ref. [12][1]. The ambipolar

[1] Devices made by Dr. Bernd Stannowski at Utrecht University

devices have been annealed 1 hour in vacuum at 180 °C before the measurements and left to cool at room temperature.

5.2.2. The methodology of the measurements

The DUTs underwent long time (24 h) electrical stress at room temperature with a positive and negative gate voltage stress of $|10\ V|$ and $|35\ V|$ named in this chapter as low and, respectively, high stress voltage. Afterwards, the TFTs were subjected to multiple stress under illumination, gate stress and temperature stress of 75 °C. The electrical parameters: threshold voltage, subthreshold swing and flat-band voltage at room temperature were recorded as a function of stress time. During multiple stress, only the change in the subthreshold swing as function of time has been presented.

The threshold voltage, subthreshold swing and flat-band voltage have been extracted from the I–V measurements and C–V measurements, respectively. Details regarding the equipment used and the way in which the threshold, flat-band voltages and subthreshold slope had been obtained, are described in Annexe of this thesis.

5.2.3. Bias stress measurements on ambipolar devices

In this section, the I–V characterisation of ambipolar devices is presented.

An ambipolar TFT shows both electron and hole accumulation under positive and negative gate voltages, respectively. The Al contact of source and drain was sputtered on top of n^+ contacts. During an annealing step at 180 ºC, Al diffuses in n^+ region allowing injection of holes from the metal contact into the channel while maintaining the conduction of electrons.

Measuring both the electron threshold voltage shift and hole threshold voltage shift help in making a distinction between the degradation mechanisms. Because of that, in the bias stress experiments of TFTs, ambipolar devices are usually preferred to unipolar TFTs.

The defect creation model states that if the Fermi level is swept to valence or conduction band, an equal number of positive and negative defects shall be created. Therefore, an equal threshold voltage shift for electrons and holes shall

appear in bias stress measurements on ambipolar devices [8]. This result is fundamental for the defect creation mechanism and distinguishes it from the charge trapping theory where no prediction about the magnitude of the shifts is made. As explained above, the defect creation model states that creation of defect states in a-Si:H results in a shift of electron and hole characteristics to the same extent, thus in equal shift of electron threshold and hole threshold [13, 14].

In the following of this section, the I_d–V_g characteristics of ambipolar TFTs are measured (fig. 5.1) and magnitude of the electron threshold voltage shift and hole threshold voltage shift resulted after gate voltage stressing the device is compared.

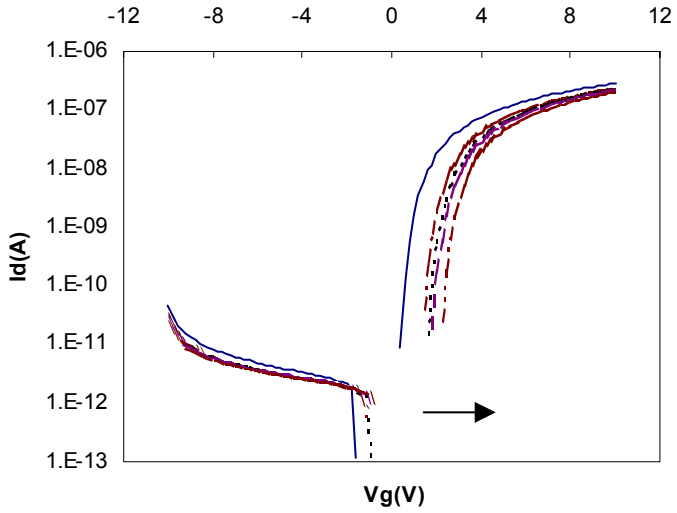

Fig. 5.1. Transfer characteristic measured initially on a fresh device and re-measured after each 3 h of gate voltage stress. The ambipolar device a-Si:H/SiN TFT (W/L = 500/100) was subjected to +35 V gate bias stress for a total time of 24 h. The arrow indicates the increasing of stress duration.

The electron threshold voltage of a fresh device was around 3 V. Apparently, the hole threshold voltage of a fresh device was larger than –20 V. The negative hole threshold voltage of ambipolar TFTs was difficult to be measured due to equipment limitation (gate voltage sweeps from minimum –40 to maximum 40 V). The I_d–V_g measurement and the equipment used are described in the Annexe of this thesis.

When subjecting the device to gate stressing, it has been noticed that the electron threshold voltage shift is not equal to hole threshold voltage shift. The shift of electron threshold voltage is bigger than the shift of hole threshold voltage. The observed inequality was reported also in ref. [12] but it casts doubt

on the assumption that the defect creation is the only degradation mechanism that alters the threshold voltage shift in a-Si:H/SiN TFTs. It is more likely that the shift is due to a combination of defect creation and charge trapping [15, 16]. Therefore, the experiments on ambipolar devices do not give straightforward answers in the debate of degradation mechanism. In the rest of the chapter only unipolar devices are used on bias stress measurements and only the electron characteristic remains for discussion.

5.2.4. Bias stress measurements on unipolar TFTs

Correlation between electrical parameters

It is known that flatband voltage V_{fb} and subthreshold swing S contribute both to the threshold voltage [17]. The change in the flat band voltage due to gate voltage stress is attributed to changes in the insulator fixed charge and interface charge whereas the changes in the subthreshold swing is attributed to changes in the bulk and interface charge in the semiconductor [18, 19]. In order to see which of these two quantities give a bigger contribution to the threshold voltage shift, many authors present either measurements of the flatband voltage shift, neglecting subthreshold swing change [20], or measurements of the subthreshold swing shift during periods of gate voltage stress and neglecting the flatband voltage shift [21].

In this section, the threshold voltage, subthreshold swing and flat band voltage have been obtained from I–V and C–V measurements that are described in the Annexe of this thesis. Afterwards these parameters have been compared and correlated.

I_d–V_g measurements at $V_g > 0$ have been performed to determine V_{th} and S before and after subjecting the device to positive and negative gate bias stress.

The V_{th} and S change were measured from I–V characteristics before and after subjecting the device to a gate bias stress. The subthreshold swing is extracted from the I–V measurements below threshold as $\left(\partial \log I_d / \partial V_g\right)^{-1}$ [22] and V_{th} as the intercept of the horizontal axis. The calculations are described in the Annexe.

It was found that the change in the subthreshold swing is positive irrespective of bias polarity (fig. 5.2) while the change in the threshold voltage

(fig. 5.3) is dependent on bias polarity. The threshold voltage induced by a positive voltage was bigger than the one induced by a negative voltage.

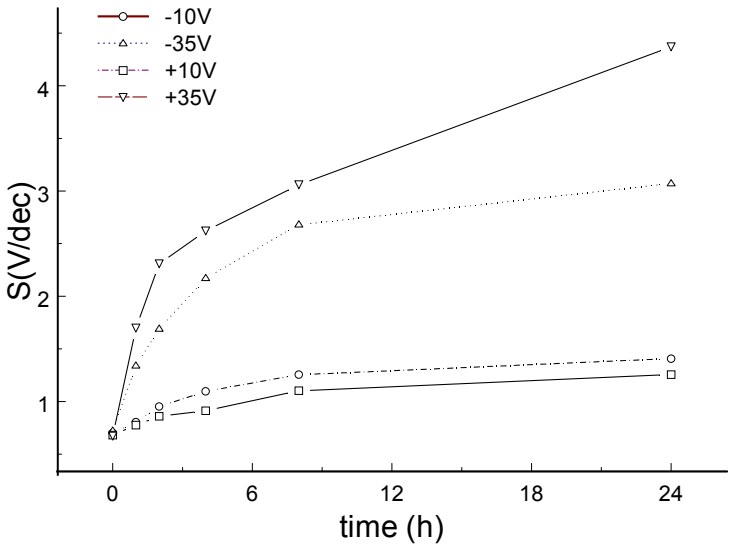

Fig. 5.2. The variation of subthreshold swing as a function of stress time at different stress voltages. (W/L = 500/100)

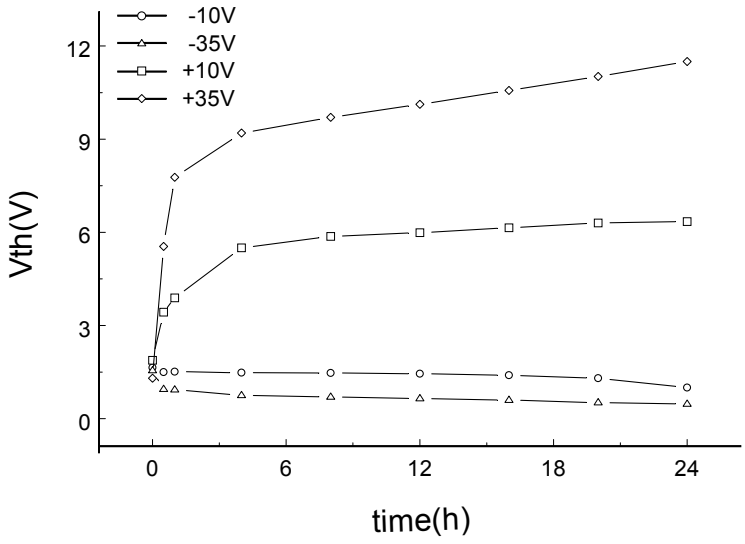

Fig. 5.3. Threshold voltage as function of time at different stress voltages (W/L = 500/100)

C–V measurements have been performed to determine V_{fb} before and after subjecting the device to positive and negative gate bias stress. It has been found that the V_{fb} shift is dependent on the polarity of the applied bias (fig. 5.4) being positive for positive bias and negative for negative bias.

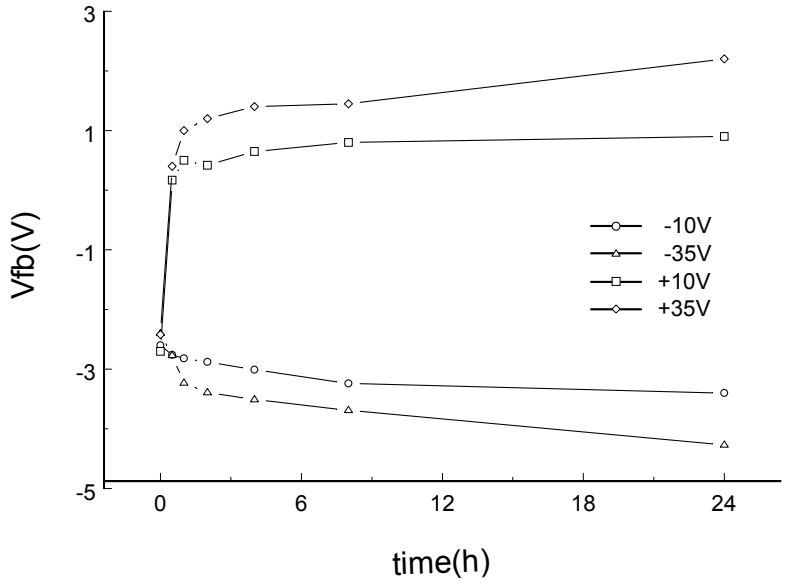

Fig. 5.4. The flat-band voltage function of time at different stress voltages (MIAS capacitors with $A = 0.025\ cm^2$)

In order to see what is the mechanism that causes the shift of the electrical characteristics under stress, the subthreshold, the flat-band voltage and the threshold voltage of the same device are correlated. I.e. for each value of the flat-band voltage, the correspondent threshold voltage is taken into account.

The flat-band voltage versus threshold voltage is shown in fig. 5.5. It can be noticed that, during positive stressing, a large change in V_{fb} is correlated with an even larger change in V_{th}. During negative stress, a small change in V_{fb} is correlated with a small change in V_{th}.

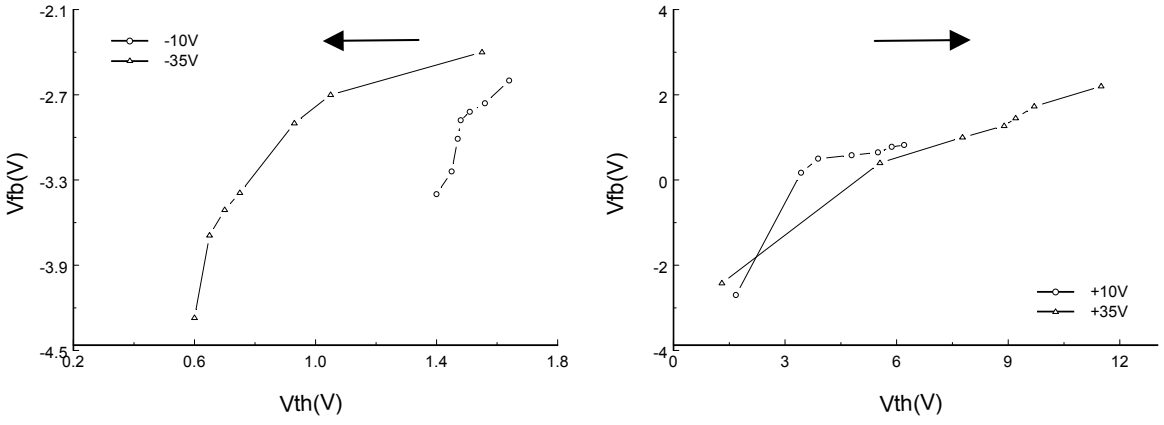

Fig. 5.5. The flat-band voltage vs. the threshold voltage. The arrow indicates the increasing of stress duration.

The change in the subthreshold swing versus threshold voltage is shown in fig. 5.6. During positive stress, a large change in the subthreshold swing is correlated with an even larger change in the threshold voltage. During the negative stress, a change in the subthreshold swing is correlated with a smaller change in the threshold voltage.

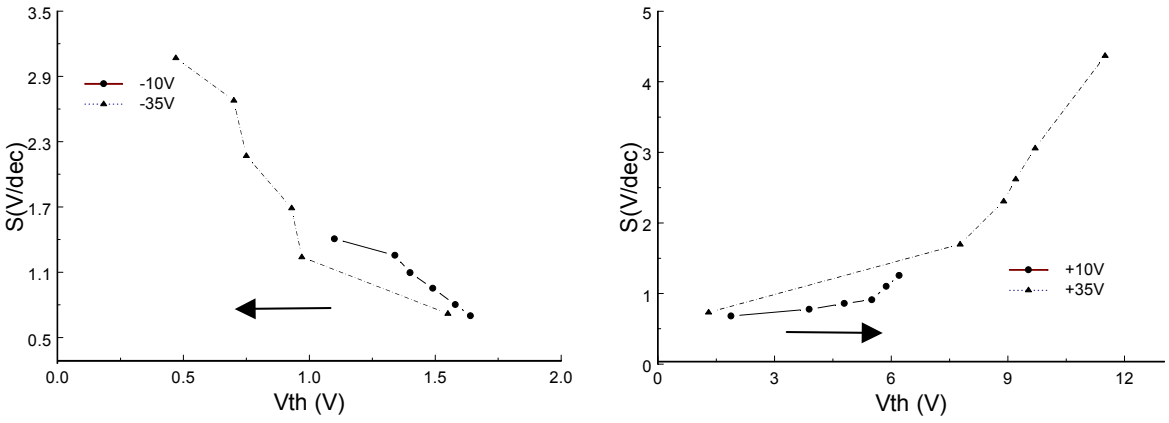

Fig. 5.6. The subthreshold swing as determined by I–V measurements versus the threshold voltage determined by I–V measurements, at the same period of stress. The arrow indicates the increasing of stress duration.

As it can be noticed from fig. 5.5 and 5.6, for long stress time, more than 4 h for example, the subthreshold swing shift and the flat band voltage shift contribute proportionally to the threshold voltage change, irrespective to the sign of applied bias. For shorter stress time, less than 1 h, the flat-band voltage changes more than the subthreshold swing during negative bias stress and it changes less than the subthreshold swing during the positive bias stress.

The positive applied gate-bias stress induces defect creation at the interface and dynamics of the defect creation at the interface is the cause for the large shift in V_{fb} and S. The negative applied gate-bias stress induces a combination of defect creation and charge trapping close to the interface. This is the cause for small shift in V_{fb} and S at low stressing voltage and relatively large change in S at high stressing voltage. At long stress time for both positive and negative stresses, it is possible that the charge trapping compete with defect creation.

Although the defect creation in a-Si:H bulk is still part of the picture, the experimental data is explained by the phenomena described above.

5.3. Conclusion

The effect of gate voltage stress on a-Si:H/SiN TFTs at room temperature has been studied by measuring and correlating the threshold voltage, subthreshold swing and flat band voltage.

The correlation helps to evaluate the contributions of the subthreshold swing and flat band voltage to the threshold voltage.

In this chapter it has been shown that a combination between defect creation and charge trapping occur during gate voltage stress. The parameters correlation shows that the interface defect creation dominates in positive stressing period and charge trapping in the transitional insulator dominates in negative stressing period.

The bias stress measurements at room temperature provide a good evaluation tool for device degradation but it is not enough to definitely conclude upon the mechanism that prevails in the degradation.

In chapter 6 is explained how this need is solved by a new method of studying the degradation. The method and the model proposed there add much to understanding the problem of a-Si:H TFTs degradation.

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CHAPTER 6

PROGRESSIVE DEGRADATION OF THIN FILM TRANSISTORS

In this chapter, another approach than classical to study the degradation in a-Si:H/SiN TFTs is proposed. The degradation is described in terms of drain current transients.

An original testing method of current transients and a model to explain the experimental data at different stress voltages and temperatures is presented.

The current transients are modelled as a consequence of a combination of defect creation and charge trapping described in the previous chapters.

6.1. Introduction

Working as a switch, the TFT is subjected to repeated stress and relaxation periods that degrade its electrical characteristics. Majority of the work regarding degradation of electrical performances of a-Si:H TFTs, when subjecting to light soaking or bias stress, focuses on the shift of the threshold voltage. The threshold voltage is extracted from I–V characteristics before and after a period of stress and the shift is calculated after each period of stress. A-Si:H TFTs are known to have a larger threshold voltage than MOSFETs and, when the threshold voltage is large, I–V characterization itself stresses the device when sweeping the gate voltage from zero to values above threshold in order to measure the drain current.

The threshold voltage degradation in a-Si:H/SiN TFTs is explained in the literature by two mechanisms: defect creation and charge trapping. The defect creation occurs in the semiconductor and the charge trapping in the insulator. The phenomena and their background of the modelling are presented in chapter 4. The defect creation is explained by the breaking of weak Si-Si bonds and dispersive hydrogen diffusion to compensate the broken bond [1]. The charge trapping is due to the charge injection from the semiconductor accumulation layer into a highly defective insulator region [2].

It has been shown in chapters 4 and 5 that there is a large debate in the literature regarding which of the two mechanisms account for the threshold voltage shift. The conclusion of the measurements of the threshold voltage performed in chapter 5 is that apparently the TFT degradation at room temperature and low bias stresses is due to a combination of interface defect creation and interface charge trapping.

In this chapter, a new method of testing the TFTs during stress is presented. In order to have a reliable estimate of the degradation of a-Si:H/SiN TFTs, different devices are subjected to positive and negative sequences of gate voltage stress and relaxation. Once applied, a voltage stress sequence is interrupted only for few seconds, at pre-selected time intervals, to allow a measurement of the source-to-drain current. The source-to-drain current, I_{sd} is measured in the linear regime at a measurement gate voltage different (lower) from the gate voltage stress. The measurements of the current are taken at minimum of time allowed by equipment. The result of undergoing cycles of positive and negative gate voltage stresses is a progressive degradation that is noticed in a transient decay and recovery of the measured current.

A new model called Progressive Degradation Model (PDM) is proposed [3] to explain the drain current transient obtained with the method introduced briefly above. The model shows that the degradation of source-to drain current during stress and subsequent relaxation is rather due to a combined effect of charge trapping and interfacial defect creation than a contribution of a single mechanism. The model achieves a consistent fit in any bias condition showing for the first time that alternative periods of stress and relaxation can be described by a continuous function of time.

Libsch [4] has done a similar study of the current transient in a-Si:H/SiN TFTs but measuring only the transients during positive gate voltage stress. He showed that after each interruption of stress and continuation of stress a slight decreasing trend of source-to-drain current I_{sd} occurred. The results were interpreted there as electron trapping within the gate insulator near the interface a-Si:H/SiN. The results of the work reported in ref. [4] are commented later on in this chapter.

6.2. Devices and Test Methodology

6.2.1. Devices under test (DUT)

Four different types of a-Si:H TFTs have been chosen for this research. The difference between them consists basically in a different insulator and a different structure. Bottom-gate TFTs with different SiN composition and TFTs with SiO_2 as gate insulator have been used. Industrial top-gate TFTs with SiN as gate insulator have also been used.

Devices with a structure Al/p type c-Si/ $SiN_{1.5}$ /a-Si:H/n^+a-Si:H/Al have been labelled here as DUT 1. The description and characterization of TFTs labelled DUT 1 is reported in [5]. These TFTs have been also used in chapter 5.

Devices with Al/n type c-Si/ $SiN_{1.2}$ /a-Si:H/n^+a-Si:H/Mo labelled DUT 2 corresponded to TFTs 3 and 4 described in chapter 2.

For comparison purposes, commercial TFTs glass/ITO/MoCr/n^+a-Si:H/a-Si:H/ N-rich SiN /MoCr were used and labelled DUT 3. TFTs with thermally grown SiO_2 as gate insulator: Al/p type c-Si/ thermal SiO_2/a-Si:H/n^+a-Si:H/Al TFT have been labelled here as DUT 4. The description and characterization of TFTs labelled DUT 4 is referred in [5].

The electrical parameters of all DUTs documented here are listed in table 6.1.

DUT	a-Si:H thickness [nm]	Insulator thickness [nm]	μ [cm^2/Vs]	V_t [V]	V_{fb} [V]
1	250	300	0.7	3.7	–2
2	250	300	0.2	3	–3.5
3	250	330	0.4	3.5	–2
4	250	150	0.17	8	–4

Table 6.1. Parameters of DUT used in this chapter

The bottom-gate DUT 2 and commercial TFTs DUT 3 were annealed at 220 °C in a vacuum for 0.5 h prior to measurement. DUT 1 and DUT 4 were annealed in a vacuum at 180 °C for 1 h. The annealing temperature was lower, only 180 °C, for DUT 1 and DUT 4 in order to avoid the degradation of the Al contacts by high temperature exposure.

For each experiment, a fresh device was used in order to avoid the effects of accumulated stress.

6.2.2. Experimental procedure

All the devices described in 6.2.1 have been subjected to the same test procedure that is to be explained in this section.

The tests are performed using 5 duty cycles. Each cycle consists of 4 alternating periods of positive stress (S+) followed by relaxation (R) and negative stress (S–) followed by relaxation (R) (fig. 6.1).

In S+ and S– the gate was forward, respectively reverse biased with the same voltage $|V_{gst}|$ while the drain was kept low at $V_d = 0.5$ V and the source was grounded at $V_s = 0$ V. In R, the three terminals were grounded.

At low V_d and zero V_s, the TFT operates in the linear regime. The linear regime prevents hot carrier effects and drain damage.

The voltage used for stress and measurement is listed in table 6.2. All the measurements have been performed using an HP4156B Parameter Analyser and the ICCAP platform program.

	S+	R+	S–	R–
stress	$V_{gst} = 25$ V $V_d = 0.5$ V $V_s = 0$ V	$V_{gst} = 0$ V $V_d = 0$ V $V_s = 0$ V	$V_{gst} = -25$ V $V_d = 0.5$ V $V_s = 0$ V	$V_{gst} = 0$ V $V_d = 0$ V $V_s = 0$ V
measure	$V_{gm} = 10$ V $V_d = 0.5$ V $V_s = 0$ V	$V_{gm} = 10$ V $V_d = 0.5$ V $V_s = 0$ V	$V_{gm} = 10$ V $V_d = 0.5$ V $V_s = 0$ V	$V_{gm} = 10$ V $V_d = 0.5$ V $V_s = 0$ V

Table 6.2. Bias value during stress and measurement

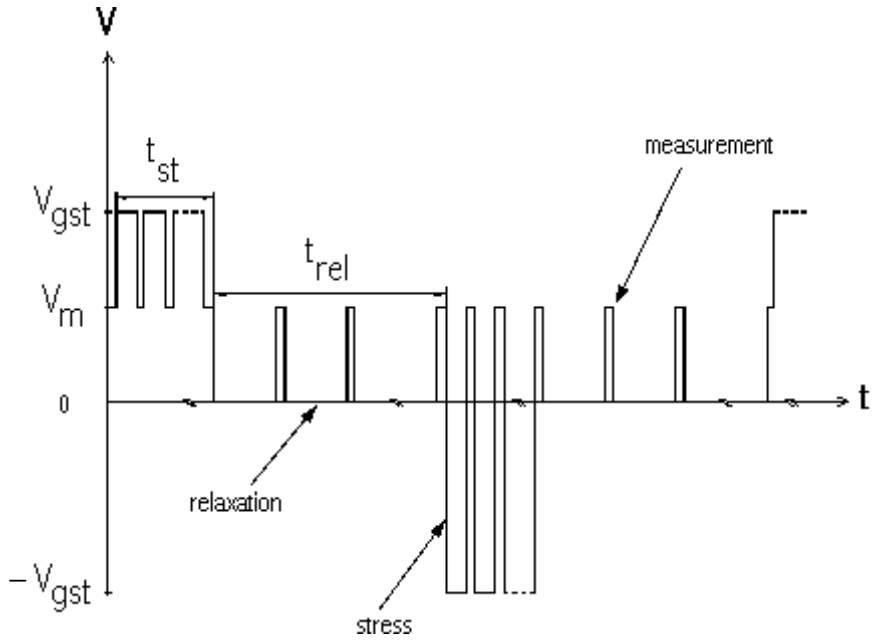

Fig. 6.1. Measurement and stress sequence used in our experiments

I_{sd} is measured at a low drain voltage to avoid the effects of hot carriers; and at a gate voltage lower than the critical voltage that might cause insulator breakdown and higher than the threshold voltage to ensure that a flow of carriers is established between source and drain.

The stress and relaxation are interrupted for a short time ($t_m \sim 2$ s), at selected time intervals (polling time, t_{poll}), in order to measure the source to drain current (I_{sd}). The selected time intervals for stressing (t_{st}) and relaxing (t_{rel}) and the time intervals between two consecutive measurements during stress and relaxation (t_{pollst} and $t_{pollrel}$) used in the experiments presented in this chapter are shown in table 6.3.

	S+	R+	S–	R–
stressing	$t_{st} = 100$ s	$t_{rel} = 300$ s	$t_{st} = 100$ s	$t_{rel} = 300$ s
polling	$t_{pollst} = 10$ s	$t_{pollrel} = 30$ s	$t_{pollst} = 10$ s	$t_{pollrel} = 30$ s

Table 6.3. Stress and relaxation time and interval between two measurements

Taking into account the measurement time at each polling, the real time spent on stressing and relaxing the device in one sequence is bigger than the selected or pre-defined time. The real stress and relaxation time in each sequence is calculated as $t_{st'} = t_{st} + \left(t_{st}/t_{pollst}\right)\cdot t_m$ and $t_{rel'} = t_{rel} + \left(t_{rel}/t_{pollrel}\right)\cdot t_m$; where t_{st}/t_{pollst} and $t_{rel}/t_{pollrel}$ give the number of measurements during stress and relaxation.

The experimental stressing time was chosen such that the device could undergo the stress for a long time, through many cycles, without damaging it. The relaxation time was chosen to be longer than stress time in order to allow the device to relax and, if possible, to reach the initial I_{sd} value before stress.

6.3. Heimann -Warfield Tunnelling Model

In this section, the Heimann-Warfield model is presented that is used later on in the modelling of current transients. Based on this model, the trap occupation functions during trapping (e.g. in S+) and de-trapping (e.g. R, S–) are derived in sections 6.3.1 and, respectively, 6.3.2.

The Heimann-Warfield model [6] describes the interface charge exchange between a semiconductor channel and insulator border traps also called switching states. In the Heimann-Warfield model, the semiconductor carriers can tunnel directly inside the insulator and move inside the insulator for a certain distance x_0 [7] before being trapped.

According to Shockley-Read-Hall statistics [8] the rate of occupation function (G) equals the fractional rates for electron capture and emission. G denotes a generic symbol for occupation function.

$$\frac{dG(E,x,t)}{dt} = \sigma(x)\cdot v_t \cdot \left(n_{sv}(t) + N_v \cdot e^{-\frac{(E-E_v)}{kT}} \right)\cdot \left(1 - G(E,x,t)\right)$$
$$- \sigma(x)\cdot v_t \cdot \left(N_c \cdot e^{-\frac{(E_c-E)}{kT}} + p_{sv}(t) \right)\cdot G(E,x,t) \qquad (1)$$

Time dependent n_{sv} and p_{sv} quantities represent the volume density of the mobile charge carriers' electrons and holes, respectively. According to an earlier model proposed by McWhorter [9], a spectrum of capture cross-sections is associated with each energy level $\sigma(E)$. Based on McWhorter's model, Heimann and Warfield derived a capture cross section decreasing exponentially with distance as $\sigma(E,x)=\sigma_0(E)\cdot\exp(-x/x_0)$ but, because $\sigma_0(E)$ is not known it was considered constant in eq. 1 and $\sigma(E,x)=\sigma(x)$. Other notations used in eq. 1 are listed in table 6.4.

v_t	Electrons thermal velocity
N_c, N_v	Effective density of states in a-Si:H conduction, valence band
x_0	Tunnelling distance
σ_0	Interface trap capture cross section
E_c, E_v	a-Si:H conduction and valence band
k	Boltzmann constant
T	Temperature

Table 6.4. Notation used in expressing the occupation functions.

Holes captured and emitted can be neglected for n type channel devices like a-Si:H TFTs. In consequence, eq. 1 will be simplified for charge exchange within the conduction band only. Therefore:

$$\frac{dG(E,x,t)}{dt}=\sigma(x)\cdot v_t\cdot n_s(t)\cdot(1-G(E,x,t))$$
$$-\sigma(x)\cdot v_t\cdot\left(N_c\cdot e^{-\frac{(E_c-E)}{kT}}\right)\cdot G(E,x,t) \qquad (2)$$

In sections 6.3.1 and 6.3.2 of the following, G is replaced by different symbols: G_c and G_e, denoting the occupation function for capture (trapping) and emission (detrapping) respectively.

6.3.1. Trapping process

It is supposed that, at $t \le 0$ when the TFT is off, all the border traps are empty and, at $t > 0$ when the TFT is on, a mobile volume charge density n_{sv} exists in a-Si:H channel. The value of n_{sv} for the measurement gate voltage ($V_{gm} = 10$ V in this chapter) is determined using the model explained in chapter 3, section 3.3. For a metal-oxide-crystalline semiconductor field-effect transistor, MOSFET, this value can be calculated according to reference [10].

Solving eq. 2 under these particular boundary conditions gives:

$$G_c(E,x,t) = F(E,t)\cdot\left(1 - e^{-\frac{\sigma(x)\cdot v_t \cdot n_{sv}(t)\cdot t}{F(E,t)}}\right) \tag{3}$$

where $F(E,t) = \dfrac{1}{1+e^{\frac{E-E_q(t)}{kT}}}$ is a step function of energy, Fermi-like function with an associated quasi-Fermi level of traps E_q defined as:

$$E_q(t) = E_c - kT\cdot\ln\left(\frac{N_c}{n_{sv}(t)}\right).$$

$F(E_q, t) = 0.5$ and E_q plays the role of a separation between states that eventually capture an electron and those that remain empty.

Knowing that $\sigma(x) = \sigma_0 \cdot \exp\left(-\dfrac{x}{x_0}\right)$, eq. 2 becomes:

$$G_c(E,x,t) = F(E,t)\cdot\left(1 - e^{\frac{-e^{-\frac{x}{x_0}+\ln(v_t\cdot n_{sv}(t)\cdot t\cdot\sigma_0)}}{F(E,t)}}\right) \tag{4}$$

For reasons that will become clear in eq. 7, the time dependent term $\ln(\sigma_0 \cdot v_t \cdot n_{sv}(t)\cdot t)$ is noted as $\frac{x_c(t)}{x_0}$ and the function $G_c(E, x, t)$ in eq. 4 becomes:

$$G_c(E,x,t) = F(E,t)\cdot\left(1 - e^{\frac{-e^{-\frac{x-x_c(t)}{x_0}}}{F(E,t)}}\right) \tag{5}$$

It easily follows that the occupation function is:

$$G_c(E,x,t) = \begin{cases} F(E,t) & \text{if } x < x_c(t) \\ 0 & \text{if } x > x_c(t) \end{cases} \tag{6}$$

According to the expression in eq. 6, the occupation function is a very step function of position; it behaves similar to the Fermi function. This observation led to the definition of a boundary between filled and empty traps. This boundary is represented by so-called capture line or tunnelling front (fig. 6.2).

$$x_c(t) = x_0 \cdot \ln(\sigma_0 \cdot v_t \cdot n_{sv}(t)\cdot t) \tag{7}$$

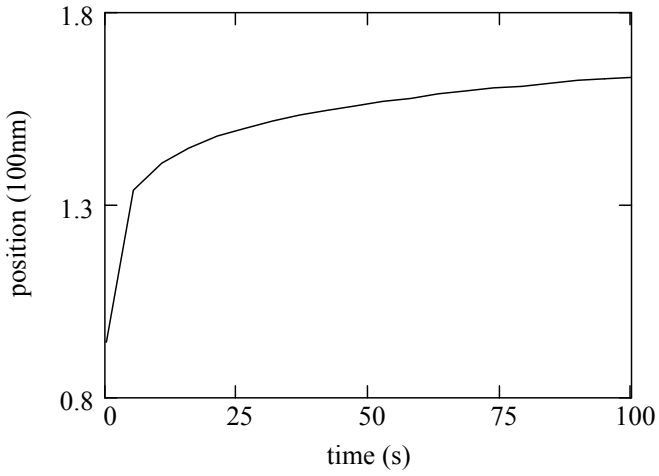

Fig. 6.2. The tunnelling front in respect with the capture time.

The capture line $x_c(t)$ separates the empty traps from the filled ones. All the traps in the area between the interface with a-Si:H, the capture line and below E_q are likely to be filled (fig. 6.3).

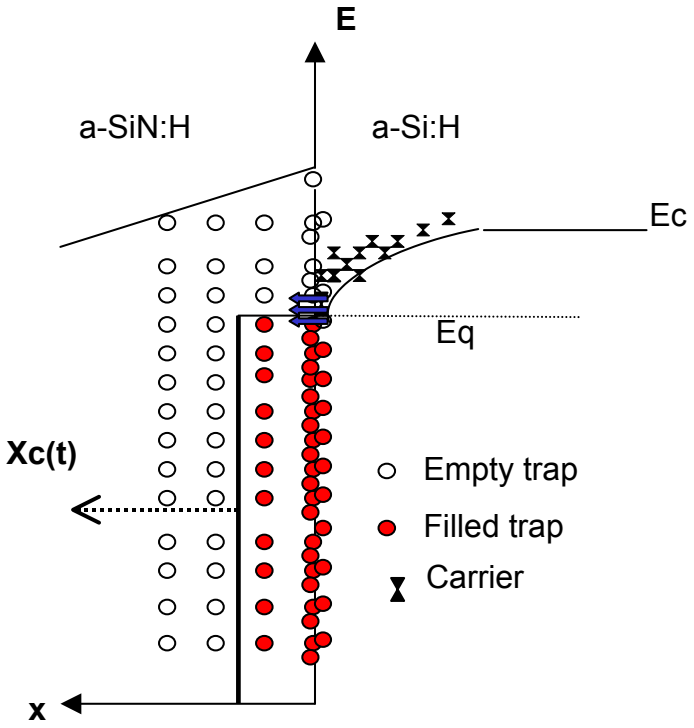

Fig. 6.3. Evolution of the capture line in time. The dotted arrow indicates the direction of the capture line movement in time. The filled arrows indicate the tunnelling of a-Si:H conduction band electrons into the SiN insulator.

6.3.2. De-trapping process

The previously filled traps start to emit their excess carriers in order to reach equilibrium. The start of de-trapping period means also the end of the trapping period and the occupation function at the beginning of detrapping is the same as the occupation function at the end of trapping $G_e(E,x,0)=G_c(E,x,t_{st})$. Solving eq. 1 under these conditions gives the occupation function in detrapping:

$$\begin{aligned} G_e(E,x,t) &= G_c(E,x,t_{st})\cdot e^{-\sigma(x)\cdot v_t\cdot t\cdot N_c\cdot e^{-\frac{E_c-E}{kT}}} \\ &= G_c(E,x,t_{st})\cdot e^{-\sigma_0\cdot e^{-\frac{x}{x_0}}\cdot e^{\ln(v_t\cdot t\cdot N_c)}\cdot e^{-\frac{E_c-E}{kT}}} \end{aligned} \tag{8}$$

Noting the term $\ln(\sigma_0\cdot v_t\cdot t\cdot N_c)-\frac{(E_c-E)}{kT}$ with $\frac{x_e(t)}{x_0}$, the occupation function in eq. 8 can be re-written as:

$$G_e(E,x,t)=G_c(E,x,t_{st})\cdot e^{-e^{-\frac{x-x_e(E,t)}{x_0}}} \tag{9}$$

Resulting in the fractional occupation function in emission:

$$G_e(E,x,t)=\begin{cases} G_c(E,x,t_{st}) & \text{if} \quad x<x_e(E,t) \\ 0 & \text{if} \quad x>x_e(E,t) \end{cases} \tag{10}$$

The function in eq. 10 is a step function similar to the function derived in eq. 6. For the same reasons as explained in 6.3.1 a time--energy dependent plane that separates the empty and filled traps is defined as:

$$x_e(E,t) = x_0 \cdot \left(\ln(\sigma_0 \cdot v_t \cdot t \cdot N_c) - \frac{(E_c - E)}{kT} \right) \tag{11}$$

The expression in eq. 11 represents the so-called emission plane or emission front (fig. 6.4).

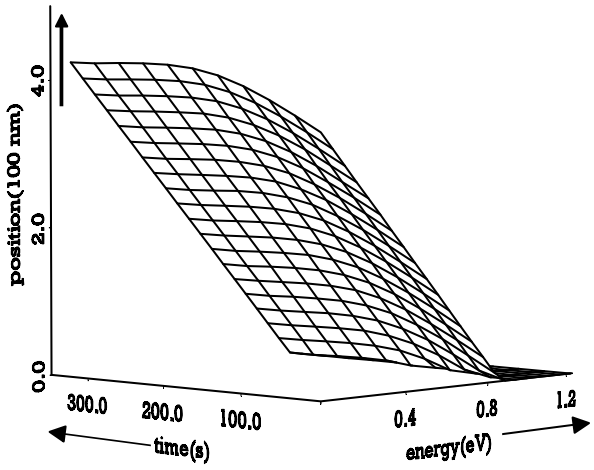

Fig. 6.4. Emission front dependency on emission time and energy.

As defined in eq. 11, the emission plane plays the role of a separation line between the traps that successfully get empty and the still occupied traps.

At a certain time t during de-trapping, all the traps situated in the area between the interface, the capture line at the end of trapping, $x_c(t_{st})$, E_q and $x_e(E,t)$ are empty (fig. 6.5).

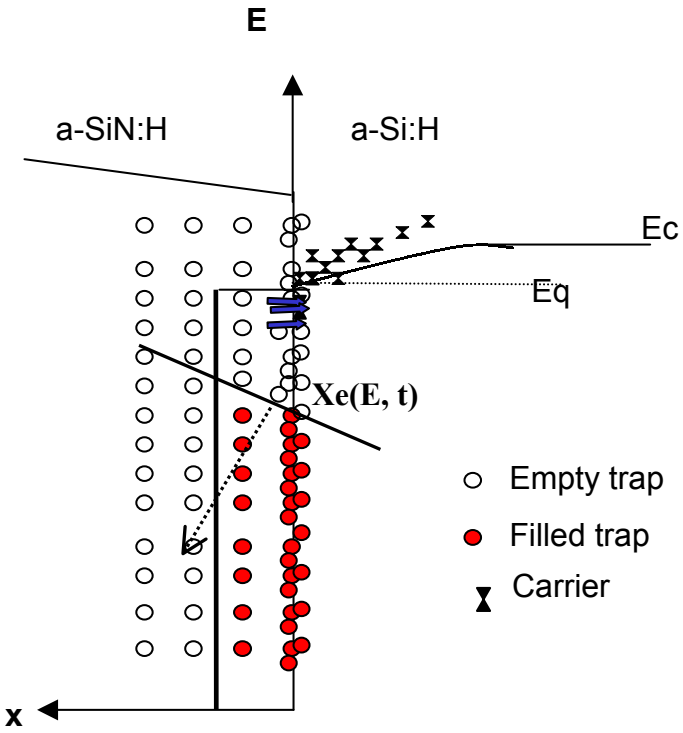

Fig. 6.5. Evolution of the emission line in time. The dotted arrow indicates the direction of emission line movement in time. The filled arrows indicate the back tunnelling of carriers from insulator border traps into the a-Si:H conduction band.

In a similar way as described in 6.3.1 and 6.3.2 the occupation functions $G_c(E, x, t)$ and $G_e(E, x, t)$ for detrapping and trapping of the carriers during S– and R after S– can be derived starting from eq. 1.

The expressions of the occupation function in trapping $G_c(E, x, t)$ and detrapping $G_e(E, x, t)$ and the capture line $x_c(t)$ and emission plane $x_e(E, t)$ are used in the modelling of the I_{sd} transients. The model is described in 6.4.

6.4. Modelling of I_{sd} transients

This section starts in 6.4.1 with a brief introduction of the classical equations that are used throughout modelling, it presents the physical explanation for the drain current degradation at room temperature and low gate voltage stress in 6.4.2 and introduces a new model called progressive Degradation Model, PDM, to explain the degradation of the current during alternating periods of stress and relaxation in 6.4.3. It is shown in 6.4.4 that PDM fits better the I_{sd} transients than other models in the literature. This section ends in 6.4.5 with considerations about the degradation of mobility and threshold voltage during positive and negative sequences of testing.

6.4.1. Classical MOSFET theory

The source-to-drain current at small V_d for TFTs and MOSFETs is described by the same formula:

$$I_0 = q \cdot \mu \cdot \frac{W}{L} \cdot n_s \cdot V_d \tag{12}$$

Where: q is the electric charge; W and L are the width and length of the device; μ is the band mobility; V_d is the drain voltage and n_s is the concentration per unit area of free conduction band electrons.

Suppose that a positive voltage is applied for a period of stress time to the gate of an n-channel MOSFET. As a consequence of stressing, the number of free carriers (electrons) accumulated in the channel decreases due to a trapping mechanism which nature is not important. Following this reasoning, the term n_s in eq. 12 decreases during stressing with a quantity $n_t(t)$ that depends on the stressing time and that represents the density of trapped carriers. $n_t(t)$ can be calculated as a product of the density of states and occupation function [11, 12].

I_{sd} decays in time when a period of positive gate voltage stress is applied on the device and eq. 12 is re-written as:

$$I_{sd}(t) = q \cdot \mu \cdot \frac{W}{L} \cdot (n_s - n_t(t)) \cdot V_d = I_0 - I(t) \tag{13}$$

Where I_0 is the current before trapping and $I(t)$ is the decrease in current due to trapping.

In a similar way, the situation of detrapping when the device is subjected to a negative stress voltage can be described. During detrapping I_{sd} will increase in time with the contribution of carriers that successfully detrapped.

A physical description of the current degradation is detailed in the following section 6.4.2 and the modelling of the experiments is explained in 6.4.3.

6.4.2. Physical description of the current degradation

When a positive gate bias is applied, for example (fig. 6.6 left), the weak Si-Si bonds that exist in a defective region close to the interface broken. The DBs defects are most probably created at the interface since there is the largest density of weak bonds resulting from the lattice mismatch between the semiconductor and the insulator. It will be explained and proven with experimental results, later on in this chapter, that the defects involved in the current degradation at room temperature are interface defects.

The channel carriers get almost instantly trapped in the created defects and, as the stress continues, more defects are created and filled.

As the Fermi level shifts closer to the semiconductor conduction band, the energy barrier between the semiconductor and the insulator lowers and, as consequence, the carriers penetrate the transitional insulator region. Some of the carriers that reach the semiconductor conduction band, tunnel directly through the crystallographic interface into the insulator, near the interface. The insulator border traps whose energy E_q is below the Fermi level are filled with electrons up to a distance from the interface that is the capture line x_c expressed in eq. 7.

Once the stress ends (fig. 6.6 right), the Fermi level moves away from the conduction band and goes below E_q. Depending on the energy of the traps and proximity to the interface, some electrons can directly tunnel back (charge back-tunnelling) to the conduction band. The traps below E_q and between the interface and emission plane x_e expressed in eq. 11 become empty.

When a voltage with reverse polarity is applied (negative bias), the surface is depleted of electrons, and holes are attracted to the semiconductor. The physical explanation for hole accumulation during negative stress is analogous to the case of electron accumulation described above.

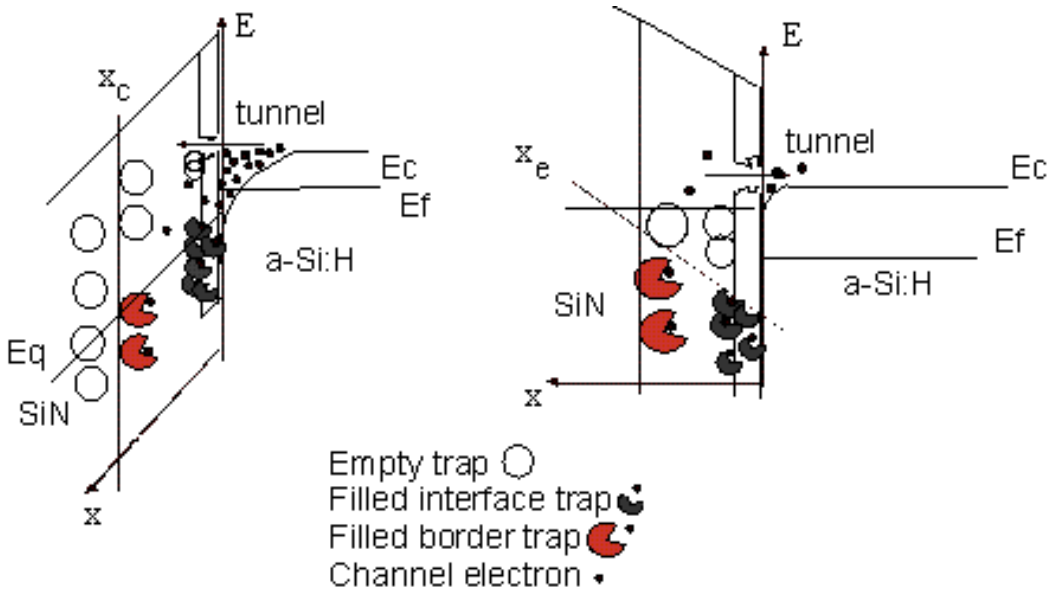

Fig. 6.6. Charge trapping in and de-trapping from states situated in a-Si:H transitional region.

6.4.3. Progressive Degradation Modelling

The Progressive Degradation Model proposed here unifies the two models of defect creation and charge trapping stating that defect creation at the interface a-Si:H/SiN and charge trapping at the interface a-SiH/SiN appear together.

Modelling of the phenomena described in 6.4.2 is presented in the following.

The following modelling assumptions were made:

1. The variation of MIS capacitance in time is negligible;
2. n^+ contacts are stable and do not degrade over time ;
3. The mobility is constant. The influence of mobility is to be discussed in sub-section 6.4.5;
4. Space-charge effects are considered negligible;
5. The interface extends from the crystallographic interface into the SiN. In this interface region are traps that exchange charges with a-Si: H channel during the experiments;
6. The capture cross section is $\sigma(x)=\sigma_0 \cdot \exp(-x/x_0)$;
7. The traps are either charged or neutral (filled/emptied);
8. The traps are uniformly distributed over energy;
9. The interface trap density decays exponentially over distance with a decay length d from the interface towards the insulator [15];
10. Interface traps can be created and reduced depending on the sign of the gate voltage [16, 17].

As a consequence of assumptions 9 and 10, the volume trap density $D(x,t)$ in a-Si:H is expressed in PDM as a function of both time and position and it is dependent on the chosen parameters D_{int} and α:

$$D(x,t)=D_0+D_{int}\cdot t^{\alpha}\cdot e^{-x/d} \tag{14}$$

D_{int} [$cm^{-3}eV^{-1}$] represents the volume density of charged interface traps. The α quantity corresponds to an increase in the interfacial charged trap density during a positive voltage stress and to a reduction in that interfacial charged trap density during a negative stress, respectively. Many papers reported an increase of the defect density during positive applied gate bias [18] and this work is extensively presented in chapter 4 and 5. Some work reported a reduction of the defects during reverse field experiments [17]. The time dispersion coefficient is

$\alpha = \begin{cases} > 0 & \text{if} \quad V_g > 0 \\ = 0 & \text{if} \quad V_g = 0 \\ < 0 & \text{if} \quad V_g < 0 \end{cases}$. D_0 is the volume density of the existing defects at the interface prior to any device history. $D_0 << D_{int}$ (~ 10^3 lower) and this quantity is neglected and kept constant throughout modelling.

The reason to introduce in the expression of $D(x,t)$ of the PDM a time dependent interface trap density lies on the defect creation model where the creation of defects is governed by power-time-dependent H diffusion. The details regarding the time dependence of defect creation and H diffusion are explained in chapter 4.

The values of D_0, α and D_{int} are determined from fitting experimental data by using MathCAD Genfit program. Genfit returns a vector containing the parameters D_0, α and D_{int} for the fitting function $I_{sd}(t)$ (eq. 14) that best approximate the data.

The parameters are extracted in pairs for a set of data, i.e. the vector (D_0, α, D_{int}) obtained after fitting the experimental data of I_{sd} in the positive stress sequence is used in the fitting of the next sequences.

At the end of the positive stress, the volume trap density is $D(x,t) = D_0 + D_{int} \cdot t_{st'}^{\alpha} \cdot e^{-x/d}$ where $t_{st'}$ is the total positive stress time with values specified in table 6.3. For fitting the negative stress sequence and the relaxation that follows after it, only the α parameter is extracted; D_{int} is the same with the one calculated for the positive stress.

A good fit for all the data obtained in the measurement sequences of the test is obtained. All the extracted parameters are within a reasonable error margin of 5 %.

The symbols and values used in modelling are summarized in table 6.4.

$d = 6 \cdot 10^{-8}\,cm$	Decay distance of the interface trap [17]
$\varepsilon_s = 10^{-12}\,F \cdot cm^{-1}$	Semiconductor permitivity [18]
$v_t = 10^{7}\,cm \cdot s^{-1}$	Electrons thermal velocity [18]
$N_c = 2 \cdot 10^{20}\,cm^{-3}$	Effective density of states in a-Si:H conduction band [18]
$n_{sv} = 5 \cdot 10^{16}\ cm^{-3}$	Volume density of mobile carriers at surface for the measurement voltage $V_g = 10$ V (calculations as described in chapter 3, section 3.3)
$x_0 = 10^{-8}\,cm$	Tunnelling distance [7]
$\sigma_0 = 5 \cdot 10^{-13}\,cm^2$	Interface trap capture cross section [19]
$E_c = 1.72\,eV, E_v = 0\,eV$	a-Si:H conduction and valence band [18]

Table 6.4. Values used in PDM.

Once it has been explained how the interface defects creation/removal is modelled in PDM, the expression of the current will be deduced based on the theory described in 6.4.1.

To do that, $I_{sd}(t)$ from eq. 13 have been adapted for the particular case of our model i.e. different expressions of the current for different polarities of the voltage stress. The adapted equations that describe the behaviour of the drain current in time will be expressed in the following for S+ and R. Similar expression can be derived for S– and R.

Trapping during positive stress, S+

During S+, in a time interval $0 < t \le t_{st'}$, where $t_{st'}$ is the total stress time, defects are created and charged and some of the conduction carriers tunnel the insulator and get trapped in the empty localized state in the transitional region up to a distance determined by the capture line at $t_{st'}$, $x_c(t_{st'})$. The transient density of trapped carriers n_{t+} is expressed as:

$$n_{t+}(t) = \int_{E_v}^{E_c} \int_{0}^{x_c(t)} D(x,t) \cdot G_c(E,x,t)\,dx\,dE \tag{15}$$

Where E_c and E_v are conduction and valence band energies in a-Si:H with values specified in table 6.4, $G_c(E,x,t)$ is the trap occupation function in S+ expressed in eq. 5; D(x,t) [$cm^{-3}eV^{-1}$] is the volume charged trap density expressed in eq. 14 with $\alpha > 0$.

Like in eq. 13, the measured source-to-drain current when subjecting the TFT to a period of positive gate voltage stress, becomes:

$$I_{sd}(t) = I_0 - q \cdot \mu \cdot \frac{W}{L} \cdot n_{t+}(t) \cdot V_d \tag{16}$$

Where I_0 is the first measured current, before S+ applied.

The fitting of the experimental data of the source to drain current with the expression in eq. 16 returns the best-fitting values of the two parameters D_{int} and α. These two values and the I_{sd} at the end of stressing time, $I_{sd}(t_{st'})$ are used in fitting of the next sequences of the test.

Detrapping in relaxation, R

During R in $t_{st'} \le t \le t_{rel'}$, some of the previously trapped carriers that are between the emission planes $x_e(E,t_{st'})$ and $x_e(E,t)$ tunnel back the insulator and participate to the conduction. The transient density of de-trapped carriers n_{tr} is expressed as:

$$n_{tr}(t) = q \cdot \frac{W}{L} \cdot \mu \cdot V_d \cdot \int_{E_v}^{E_c} \int_{x_e(E,t_{st'})}^{x_e(E,t)} D(x,t_{st'}) \cdot G_e(E,x,t-t_{st'}) dx dE \qquad (17)$$

Where $G_e(E,x,t-t_{st'})$ is the trap occupation function in R as expressed in eq. 10; $D(x,t_{st'})$ is the charged trap density after S+. No defects are created during R therefore $\alpha = 0$. Because no defects are created when the device relaxes there is no fitting in R that follows S+. The value of D_{int} in R is $D_{int} \cdot t_{st'}^{\alpha}$, where D_{int} and α are the result of fitting in S+.

The source-to-drain current that has been measured at the end of previous period of stressing increases due to the detrapping and it is expressed as:

$$I_{sd}(t) = I_{sd}(t_{st'}) + q \cdot \mu \cdot \frac{W}{L} \cdot n_{tr}(t-t_{st'}) \cdot V_d \qquad (18)$$

Where $I_{sd}(t_{st'})$ is the last value of the fitted current in S+.

In the light of eq. 16 and 18, I_{sd} is modelled as a time-continuous function for the periods of time corresponding to positive stress S+, relaxation R and negative stress S–.

The expressions of $I_{sd}(t)$ during a negative voltage stress followed by a relaxation are similar with the expressions in eq. 16 and 18. They can be easily derived following the same reasoning as above taking into account that:

- The charged interface trap density evolves in time according to eq. 15, with a dispersion coefficient which sign depends on the sign of the applied voltage;
- In each sequence of the test, D_{int} depends on the D_{int} calculated at the beginning of the cycle and only α remains a parameter in each sequence.

For one cycle, the modelled $I_{sd}(t)$ is presented in eq. 19.

$$I_{sd}(t)=\begin{cases} I_0 - q\cdot\dfrac{W}{L}\cdot\mu\cdot V_d\cdot\displaystyle\int_{E_v}^{E_c}\int_{0}^{x_c(t)} D(x,t)\cdot G_c(E,x,t)\,dx\,dE & \text{if } 0<t\le t_{st'} \\ I(t_{st'}) + q\cdot\dfrac{W}{L}\cdot\mu\cdot V_d\cdot\displaystyle\int_{E_v}^{E_c}\int_{x_e(E,t_{st'})}^{x_e(E,t)} D(x,t_{st'})\cdot G_e(E,x,t-t_{st'})\,dx\,dE & \text{if } t_{st'}\le t\le t_{rel'} \\ I(t_{st'}+t_{rel'}) - q\cdot\dfrac{W}{L}\cdot\mu\cdot V_d\cdot\displaystyle\int_{E_v}^{E_c}\int_{0}^{x_c(t)} D(x,t_{st'}+t_{rel'})\cdot G_c(E,x,t-(t_{st'}+t_{rel'}))\,dx\,dE & \text{if } t_{rel'}<t\le t_{st'} \\ I(2\cdot t_{st'}+t_{rel'}) + q\cdot\dfrac{W}{L}\cdot\mu\cdot V_d\cdot\displaystyle\int_{E_v}^{E_c}\int_{x_e(E,2\cdot t_{st'}+t_{rel'})}^{x_e(E,t)} D(x,2\cdot t_{st'}+t_{rel'})\cdot G_e(E,x,t-(2\cdot t_{st'}+t_{rel'}))\,dx\,dE & \text{if } t_{st'}<t\le t_{rel'} \end{cases} \tag{19}$$

An example of fitting I_{sd} transients for 5 cycles of degradation is shown in fig. 6.7.

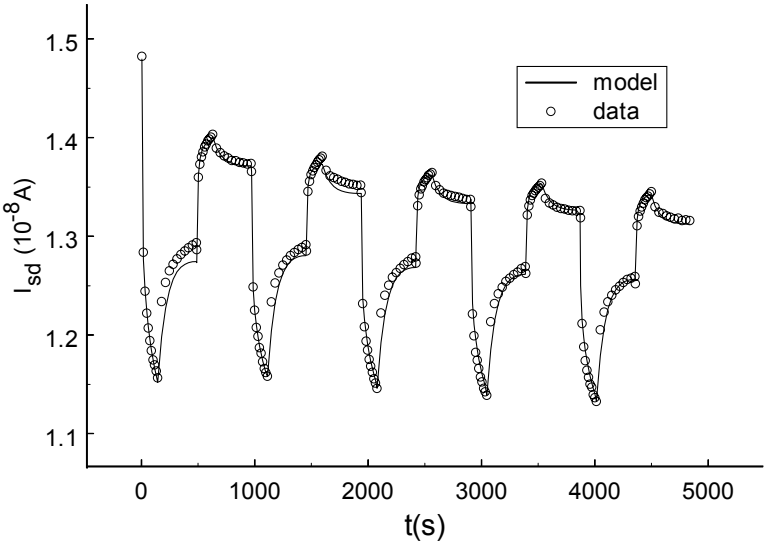

Fig. 6.7. Test with 5 cycles (V_{gst} = 25 V at T = 293 K) of DUT 3 TFT. The values of time and bias used in the experiment are listed in table 6.2 and 6.3.

The results of testing of the three DUTs described in table 6.1 are shown in fig. 6.8.

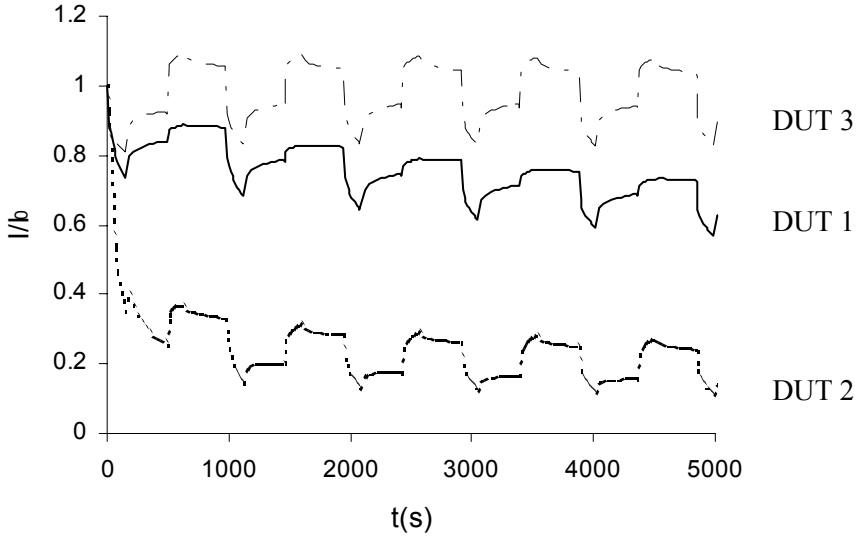

Fig. 6.8. Normalized currents during S+/R/S–/R sequence over stress time for DUT 1, 2 and 3.

The results of fitting the experimental data of S+/R/S–/R test for each DUT which transients are shown in fig. 6.8, are presented in table 6.5.

DUT/cycle	D_{int} [$cm^{-3}eV^{-1}$]·10^{18}	α (S+)	α (S–)
DUT 1			
1	4.51	0.17	–0.45
2	2.77	0.29	–0.38
3	2.7	0.3	–0.5
4	2.5	0.3	–0.5
5	2.2	0.3	–0.5
DUT 2			
1	1.8	0.21	–0.01
2	0.45	0.32	–0.01
3	0.4	0.32	–0.01
4	0.38	0.34	–0.01
5	0.36	0.36	–0.01
DUT 3			
1	0.33	0.2	–0.7
2	0.16	0.25	–0.68
3	0.14	0.26	–0.66
4	0.13	0.27	–0.58
5	0.13	0.27	–0.56

Table 6.5. Values of the parameters D_{int} and α calculated in PDM for S+/R/S–/R test.

6.4.4. Fitting I_{sd} transients with other models in the literature

In this section it is shown that PDM gives the only satisfactory fit for both positive and negative stressing sequences of the testing.

In fig. 6.9 the positive and negative stress periods in the first test cycle applied on the commercial DUT are zoomed and fitted with three models: two state-of-the-art models and PDM proposed in this thesis. The two state-of-the-

art models are described in chapter 4: the charge trapping and the defect creation. The dispersive equation has been used for the charge trapping and the stretched exponential for defect creation; both equations have been derived in chapter 4. In addition, a fitting using PDM was shown. All three models fit the experimental data in the positive stressing but not in the negative stressing period. Only PDM gives a good fit of the data in the negative stressing.

In the fit shown in fig. 6.9 for the first cycle of degradation of DUT 3, after S+, the current, I_{sd} is with 78 % smaller than the initial value, I_0; after R it is smaller with 87 % so, it recovers only 10 %; after S– it is with 95 % smaller than I_0 recovering 8 % and, finally, after another R, the value of I_{sd} is with 92 % smaller than I_0.

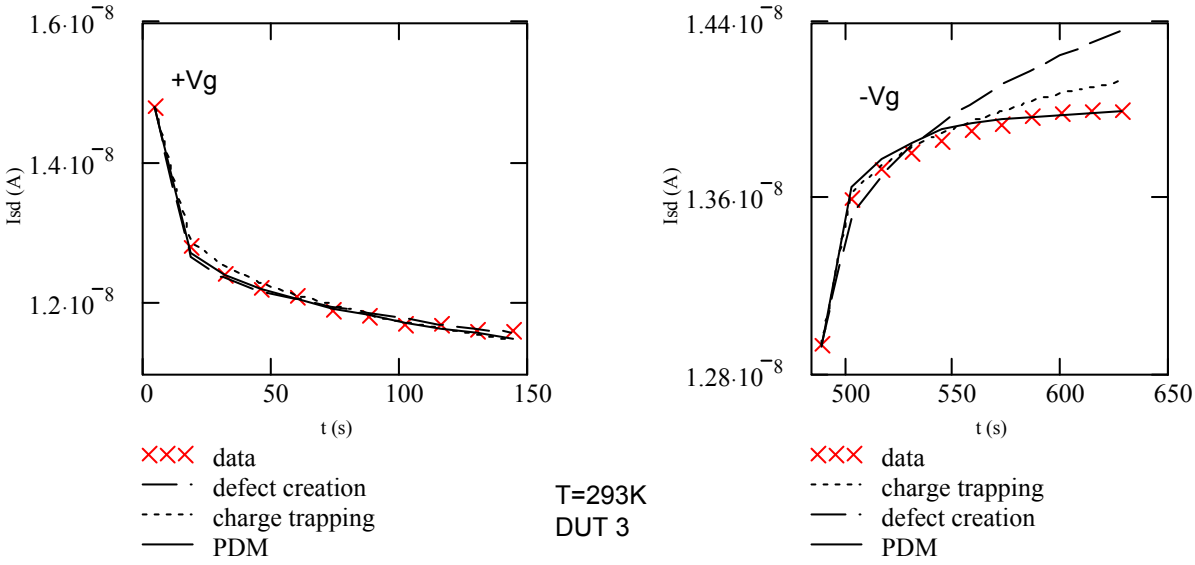

Fig. 6.9. Current decay during positive gate voltage stress (left) and current recovery during negative gate voltage stress (right) fitted by equations describing the defect creation and charge trapping models presented in chapter and PDM. Relaxation is not shown in the figure. The testing parameters: voltages and time are listed in tables 6.1 and 6.2.

In order to see whether the positive stressing period was too short to allow a distinction between the models, measurements up to 10^4 s, at +30 V gate bias stress, have been performed as well. The results were similar to the results obtained for shorter stress times in the sense that prolonging the stress time did not cast more light into the ambiguity and gave a transient that fits both degradation models.

6.4.5. Mobility and threshold

In this section, the mobility and threshold voltage degradation of a-Si:H/SiN TFTs is investigated using a simple method that makes use of S+/R/S−/R testing method.

One of the hypotheses of PDM is that the mobility remains constant throughout the testing. However, I_{sd} is influenced by both changes in mobility and threshold voltage. Above threshold, most of the charge resides in the interface states, the amount remaining for conduction is dramatically reduced. The large trapped charge gives rise to Coulomb scattering that reduces the mobility of the remaining free carriers. The net result is a dramatic reduction in the current, or equivalently, a dramatic increase in the specific on-resistance of the channel.

The same S+/R/S−/R testing method as described in section 6.2.2 has been used to investigate the mobility and threshold voltage behaviour during positive/negative stressing.

I_{sd} transients during S+/R/S−/R test have been measured at two slightly different gate voltages V_{gm1} and V_{gm2}. I.e. two consecutive measurements of the current were performed at a different gate voltage. There are only 2 s differences between two consecutive measurements; that is the pausing time necessary for the measurement itself. Thus at each 2 s, two sets (I_{sd1}, V_{gm1}) and (I_{sd2}, V_{gm2}) are obtained.

The gate voltage stress was the same for both measurements and its value is not important for the determination of mobility or threshold.

From this point, the calculation of threshold and mobility make use of the same method of determination like I–V characterization that is extensively described in the Annexe. In I–V characterization, the gate voltage is swept in steps from 0 to a certain value well above threshold. The I_{sd} currents are recorded at each V_g step in pairs such as (I_{sd1}, V_{g1}), (I_{sd2}, V_{g2}) and so on till the last value of V_g. The mobility and threshold are determined from the intercept and slope of I–V graph. The values of the measurement gate voltage V_{gm1} and V_{gm2} are close enough to approximate an imaginary I–V curve between these two points with a line and to calculate mobility and threshold. Applying this method to the pairs (I_{sd1}, V_{gm1}) and (I_{sd2}, V_{gm2}) obtained doing two

S+/R/S−/R tests, the mobility and threshold are obtained as:

$$\mu \sim \frac{I_{sd1} - I_{sd2}}{V_{gm1} - V_{gm2}}$$

$$V_{th} \sim \frac{V_{gm1} \cdot I_{sd2} - V_{gm2} \cdot I_{sd1}}{I_{sd2} - I_{sd1}}$$

Calculating the mobility at each time during S+ and S− sequences, it appears that the mobility does not change significantly over time (fig. 6.10) and it can be considered constant (only 4 % degradation of mobility).

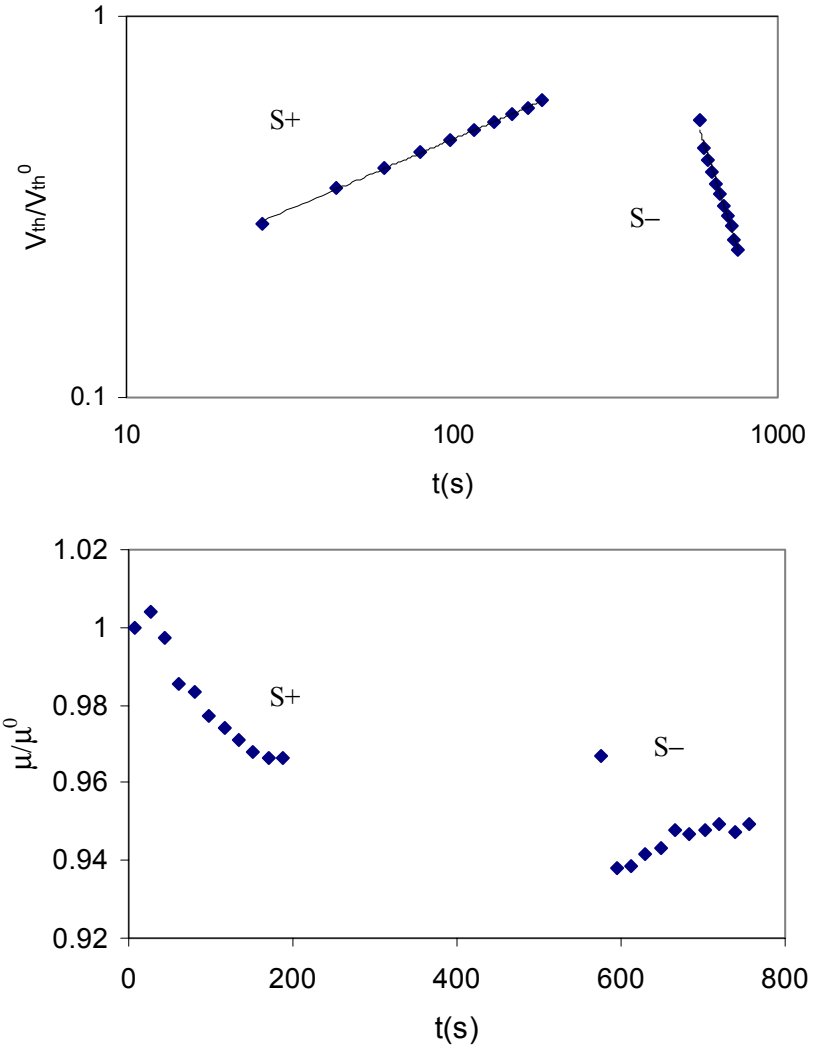

Fig. 6.10. Normalised threshold (log log scale) and mobility versus time for positive and negative stress periods at $V_{gst} = 20$ V with $V_{gm1} = 8$ V and $V_{gm2} = 10$ V. DUT 1 TFT.

The very small mobility degradation indicates that there is not much scattering on the interface defects. The fluctuation of mobility is due mainly to the light roughness of the interface [20].

A stretched-exponential dependence of the threshold voltage on the stress time for positive and negative stress is obtained as $\ln(V_{th}) \sim t^x$ [20]. The stretched exponential behaviour of the threshold voltage was also confirmed by I–V measurements over long stress times as shown in chapter 5.

Considering the results above, the current degradation in a-Si:H/SiN TFTs is not much influenced by the changes in mobility but it is rather the consequence of the changes of threshold voltage.

6.5. Discussion regarding the progressive degradation of TFTs

It has been shown in the literature that the interface between a-Si:H and SiN has a high density of defects resulting in significant band bending even when no stress is applied to the device [21, 22]. The band bending is higher when a sub-stoichiometric SiN is used as gate dielectric [23]. When a gate voltage stress is applied to a TFT with a sub-stoichiometric SiN, the channel carriers penetrate into SiN due to the band bending and, as stress time increases, a space charge is built up affecting the strength of the electric field at the interface.

It has been also shown in the literature that creation of defects is more severe in a TFT with low quality a-Si:H or γ-a-Si:H [24]. It is considered that a gate stress at room temperature changes only the occupancy of the states in a-Si:H but the density of the defects does not change [25]. Contrary, some research shows that the defect creation actually appears in bias stress measurements at room temperature [26].

Summarizing from section 6.2, the devices used for testing in this thesis chapter are TFTs made with above-stoichiometric SiN or N-rich SiN (DUT 1 and 3) and sub-stoichiometric SiN or Si-rich SiN (DUT 2). The quality of deposited a-Si:H is considered to be the same for DUT 1 and 2. DUT 1 and 2 are bottom gate TFTs and DUT 3 is a top gate TFT. For all three DUTs the deposited a-Si:H is considered high quality or α-a-Si:H.

According to the literature, DUT 2 TFTs shall be affected more by degradation due to charge trapping than DUT 1 and 3 that are with N-rich SiN. The degradation due to defect creation shall be equal to all three DUTs.

In this chapter the results of the testing of these three DUTs are discussed.

6.5.1. The transient nature of the currents

After subjecting the TFTs to cycles of repetitive stress and relaxation by using the testing method presented in section 6.2.2, a fast decay of the current followed by a slow decreasing trend of the current appears. In fig. 6.12 are shown the values of I_{sd} for a device subjected to S+/R/S–R test for 5000 s. It can be noticed in this example that the first I_{sd} values in S+ of each cycle gives a fast decaying trend, resembling a logarithmic decay, whereas the last I_{sd} values in S+ of each cycle gives slow trend, apparently linear trend. This behaviour is due to the existence of two processes: a fast one during positive stress and a slow one after cycles of stressing.

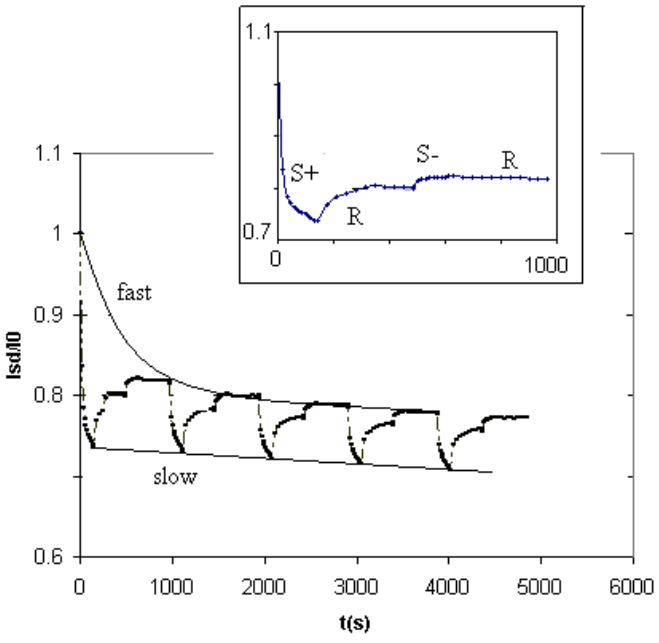

Fig. 6.12. The transient pattern of DUT 1 (zoom in the first cycle showing the current behaviour during alternating period of stress). The testing time and voltages that are used in the experiment are listed in tables 6.1 and 6.2.

It appears that the first period of positive stressing causes the most severe current degradation whereas the next cycles causes less degradation. Particularly in the first 10 s of S+, 20 % degradation of the current occurs whereas during the next 90 s of S+, the current degrades only 5 % in respect to the current value measured prior to stressing (fig. 6.12). Thus, the most degradation of current is noticed in the first seconds of positive stressing comparing to the following seconds. In the literature a fast process like this is related to the interface states creation [27]. If the defects would have been created in the a-Si:H bulk, a longer time would have been necessary to fill them with carriers from the channel.

In terms of PDM, the values of parameters D_{int} and α reflect the discrepancy between the first cycle and the next cycles. α in the S+ of the first cycle is around 0.2 for all the devices; it increases in the S+ of the next cycles and stabilizes around 0.3 (table 6.5). The lowest increase of α is for DUT 3 that appears to have also the smallest I_{sd} degradation comparing to DUT 1 and 2 (fig. 6.9). D_{int} decreases from the value calculated in the first cycle. Apparently, α itself is not related to the stoichiometry of SiN gate insulator but the way in which it varies between cycles is related to the quality of the insulator. I.e. α increases less between first and second cycle of DUT 1 and 3 that are N-rich than in DUT 2. On the other hand, α varies only a little throughout the S-sequences of a single DUT but it is different from device to device as like some devices succeed in recovering more than the others. E.g. for DUT 2 the dispersion coefficient for S– is a very small value ~ –0.01. Because in DUT 2 the current degrades faster than it recovers, I_{sd} degrades more rapidly than in the other two devices.

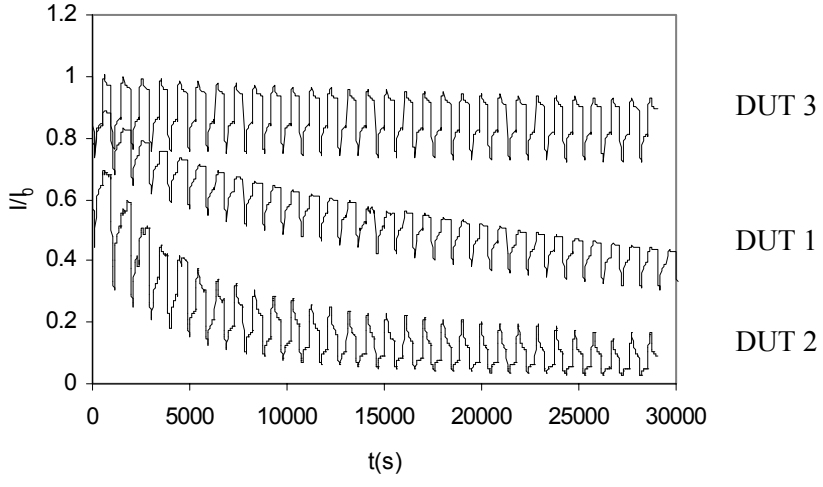

Fig. 6.13. Normalized current for long time stress at 25 V gate bias.

When subjected to $3 \cdot 10^4$ s (fig. 6.13) of alternative stress and relaxation instead of $5 \cdot 10^3$ s (fig. 6.12), it appears that the fast decaying trend is neither logarithmic nor power-like and the slow decaying trend is not linear for all the devices. The experiments performed up to 30 cycles of alternative stress show that DUT 3 has the smallest decay of current during the first S+ period; these devices reach sooner stable values of the drain current than DUT 1 and 2 (fig. 6.13). The DUT 1 seems not to reach stabilization in this time frame. For DUT 2 an apparent 'linear' trend is reached after 8 cycles. Is indeed common for all DUT that, after the 2nd cycle, the current decaying trend 'slows' down so much that becomes almost linear for some devices like DUT 3 and 2 but this is not the case for DUT 1 (fig. 6.13).

In terms of PDM, after the 2nd cycle, the value of the D_{int} and α in both S+ and S– sequences do not change significantly over time meaning that the creation of fast interface defects ceased; there is only a change in the occupancy of defects in each cycle of test. An overall picture of the degradation of the I_{sd} shows that by each cycle of S+/R/S–/R test, I_{sd} slowly and progressively degrades. The slow trend that appears in most devices after periods of alternating stress an relaxation is not a clear linear one as it would be the case if only the defect occupancy changed by time but it goes very slowly down indicating two possible explanations: 1. an amount of available channel charge remains irreversibly trapped in SiN after each cycle of test and 2. defects in the bulk of a-Si:H are created.

In order to see whether the order of stress sequences matters, the effect of reversing the stress sequences has been investigated in section 6.5.2.

6.5.2. Reverse bias sequence

The transients of two TFTs have been measured in S+/R/S–/R sequence and in the reverse sequence S–/R/S+/R (fig. 6.14). Reversing the bias sequence does not change the behaviour of I_{sd} in each sequence in the sense that the current decays in S+ and recovers in S– in both test. As can be seen in fig. 6.14, the current decays and recovers more in the first cycle in S+/R/S–/R test than in S–/R/S+/R but, in the other cycles the current pattern looks similar for both tests.

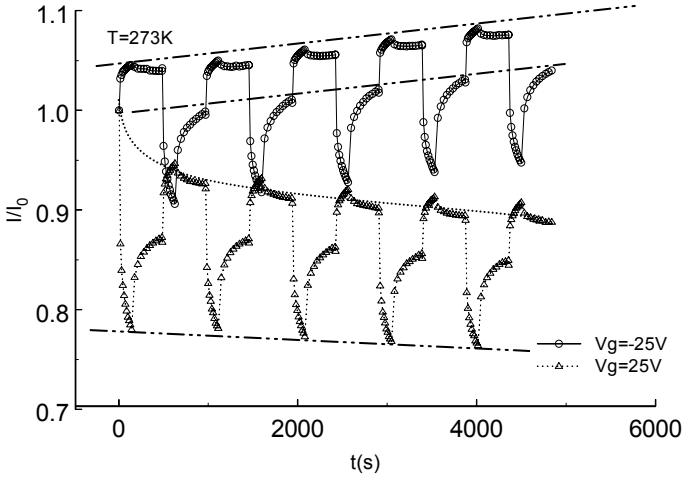

Fig. 6.14. Reverse test S–/R/S+/R (circles) and forward test S+/R/S–/R (triangles). The experiments have been performed on DUT 3 at room temperature with the testing time and voltages listed in tables 6.1 and 6.2. The trends are indicated with dotted lines.

In other words, this result points out that changing the order of S+ with S– does not result in a degradation of I_{sd} in S+ as fast as or faster than that in S+ in S+/R/S-/R test. At the end of the first S+ in S–/R/S+/R test, I_{sd} is with 90 % smaller than I_0 comparing to the end of first S+ in S+/R/S-/R test where I_{sd} becomes with 78 % smaller than I_0.This result contradicts the conclusion of the work refereed in [28] claming that the charge trapping in SiN under positive bias increases when SiN is previously depleted by a negative bias.

The I_{sd} trend in S–/R/S+/R cycle looks like increasing smoothly and slowly, symmetrical to the slow trend in S+/R/S–/R test.

The first period of S– in the reverse test sequence appears to help the device to 'stabilize' the current. This is possible because S– plays the role of 'annealing' of defects, or recovery of the defects as modelled in PDM. In consequence, the current does not degrade during S+ as much as in S+/R/S–/R test and the device can recover more of the initial value of the current.

The fitting of experimental data in the reverse test goes in the same way like the fitting described in section 6.4.2 for S+/R/S–/R test.

6.5.3. a-Si:H/SiO_2 TFT and a comparison with a-Si:H/SiN TFT

Applying the S+/R/S−/R test to a-Si:H /SiO_2 TFTs, DUT 4, resulted in a current decaying during S+ and S− and recovering only in relaxation (fig. 6.15). The current decay and no recovery during S− is expected in a-Si:H/SiO_2 TFTs because a positive threshold shift for both negative and positive polarities of stress is obtained and this translates into I_{sd} decaying during both S+ and S−. The current decay during S− in the first cycle is the most severe one comparing to the decay in the next cycles. During S+, I_{sd} decay is similar to the I_{sd} featured in DUT 1-3.

In the first cycle, at the end of S+, I_{sd} value is with about 95 % smaller than the initial value I_0 but the decay at the end of first applied period S− is about 30 % smaller than I_0. The S− periods in the next cycles have a less severe impact on the current decay comparing to the first period with negative polarity of gate voltage stress whereas the positive polarity of the gate voltage stress does not have a major influence in the decaying trend. After the 1st cycle, the decay during S− becomes smaller and, after the 3rd cycle, the device appears to stabilize, in terms of current transients, to very low values of current, with about 15 % smaller than the initial value.

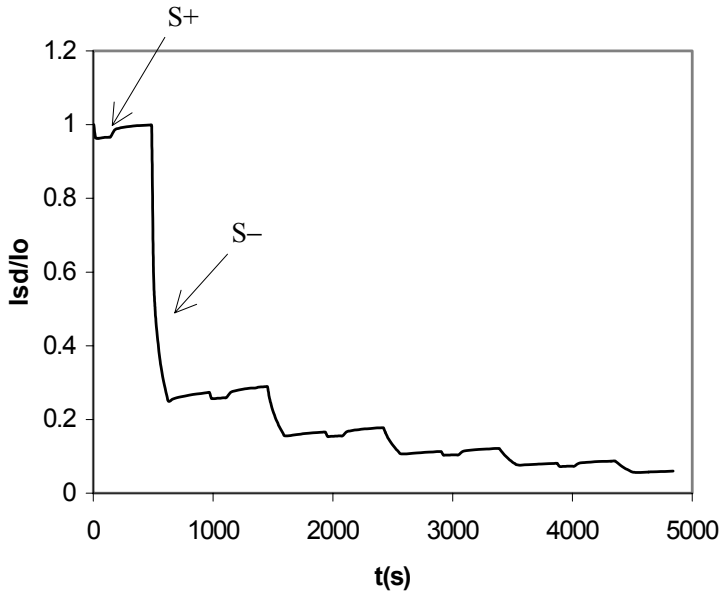

Fig. 6.15. Normalised transient current for a-Si:H/SiO_2 TFT subjected to S+/R/S−/R test at room temperature.

Hence, it appears that the negative applied bias causes much more degradation of I_{sd} than the positive stress, exactly opposite of a-Si:H/SiN TFTs. Moreover, the current degradation in the first applied S– to DUT 4 appears to be much more significant than the current degradation in the first applied S+ to DUT 1-3.

Two explanations are possible for this: 1. defects are easier created in DUT 4 then the other DUT; 2. charge exchange between the channel and the border traps is easier in DUT 4. When SiO_2 is thermally grown on c-Si substrate there is virtually no charge trapping in the gate insulator. However, on one hand, it was reported that depositing a-Si:H on SiO_2 resulted in a rough and voided interface [29] and this fact favours explanation 1. On the other hand, the charge exchange between the a-Si:H channel and the border traps in thermally grown SiO_2 has been proven to exist by different authors as it will be discussed in chapter 7, section 7.2; this fact favours explanation 2.

The differences between the degradation in a-Si:H/SiN TFTs and a-Si:H/SiO2 TFTs are explained in the following, in the light of the defect pool model that is described in chapter 2 for a-Si:H/SiN TFTs.

SiN induces an electron accumulation layer in a-Si:H raising the Fermi level towards the conduction band. Thus, the equilibrium distribution of states has more D^- defects in the lower part of a-Si:H band gap. On the other hand, SiO_2 induces an electron depletion layer in a-Si:H, lowering the Fermi level towards the valence band. Thus, the equilibrium distribution of states has more D^+ defects in the upper band gap. In other words, fixed negative charge in SiO_2 give rise to a density of D^+ states higher in the upper band gap of a-Si:H whereas fixed positive charge in SiN give rise to a higher density of D^- states in the lower gap of a-Si:H. The effect of a period of positive gate stressing on an both a-Si:H/SiO_2 and a-Si:H/SiN TFTs is creation of D^- defects. The effect of a period of negative gate stressing on an a-Si:H/SiO_2 TFT, is creation of D^+ defects, whereas the negative stress on a-Si:H/SiN mainly reduces D^- defects.

However, the defect creation model alone does not explain why the current degradation induced by a stress with the same magnitude only with negative polarity in a-Si:H /SiO_2 TFT and positive polarity in a-Si:H/SiN TFTs is higher in the first case than in the second case.

Reversing the bias sequence i.e. starting with S– instead of S+, the decay of I_{sd} is even more dramatic, the current after the 2^{nd} cycle being with 5 % smaller than the initial value I_0 (fig.6.16).

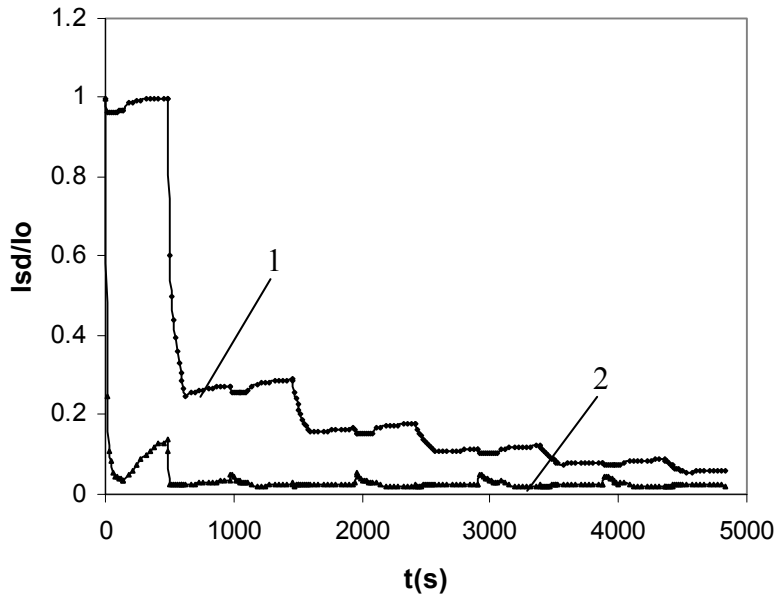

Fig. 6.16. Normalized currents vs. time for 1. S+/R/S–/R and 2. S–/R/S+/R tests, both performed at a stress voltage with magnitude 25 V for the same periods of time as in table 6.2.

The decrease in mobility overtime for a-Si:H /SiO_2 devices is higher than for a-Si:H/SiN devices. Since the a-Si:H quality is considered the same for nitride insulator and oxide insulator device [5], the difference in mobility degradation is explained by different interface qualities.

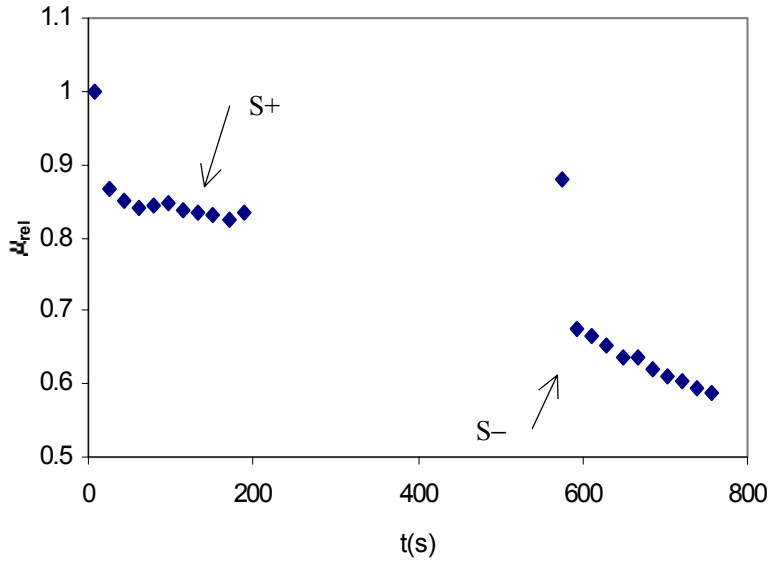

Fig. 6.17. Relative mobility vs. time for positive and negative stress periods at V_{gst} = 35 V with V_{gm1} = 32 V and V_{gm2} = 30 V

The mobility degradation in time is significant for a-Si:H /SiO_2 TFT as it can be seen in fig. 6.17. This result is in agreement with the considerations of reference [29] regarding the rough interface between a-Si:H and SiO_2 and thus, the higher mobility degradation in stressed a-Si:H/SiO_2 TFTs than in a-Si:H/SiN TFTs. The threshold voltage changes in time according to $\ln(V_{th}) \sim t^x$ (only at different x than in a-Si:H/SiN TFTs).

Considering the results above, it results that, in DUT 4, the mobility as well contributes to the current degradation.

$I_{sd}(t)$ appeared to obey a power-law time decay for S+, similar for both TFTs but the entire sequence of I_{sd} function of time could not be fitted to our model for S– because of three factors: 1. the abrupt decay of the current in the first period of S– that makes difficult to find a matching pair of D_{int}, α parameters to characterize one cycle; 2. because the mobility cannot be considered constant as supposed in section 6.4.3 and 3. assuming a time dependent mobility during stressing complicates the fitting procedure and MathCAD is not appropriate to solve such complex equations.

6.5.4. Experiments at Different Biases and Temperatures

According to the literature, the defect creation is temperature dependent whereas the charge trapping is less dependent [30]. But there are also papers explaining that charge trapping can be temperature sensitive as well [31, 32].

Because the temperature of the ambient and the bias stress are so important to distinct between the two mechanisms, a large number of experiments at different gate voltage stress and ambient temperature have been performed. The ambient temperature was the temperature of the chuck and it was varied in the range of 273 K to 343 K using Temptronic Temperature Controller as described in the experimental techniques chapter.

It was found that the current transient depends on the applied stress and ambient temperature as evidenced by the results presented in fig. 6.18 and fig. 6.19. The current is sensitive to temperature and applied bias stress.

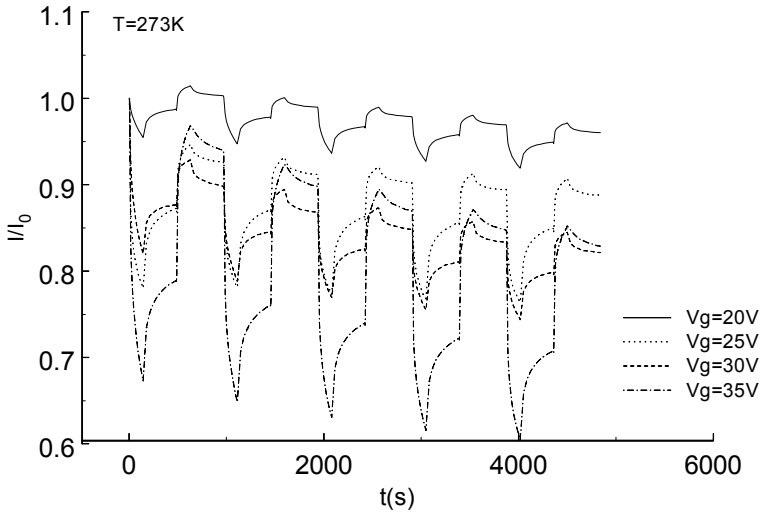

Fig. 6.18. Tests performed at the same temperature (T = 273 K) and different gate bias using DUT 3 TFTs.

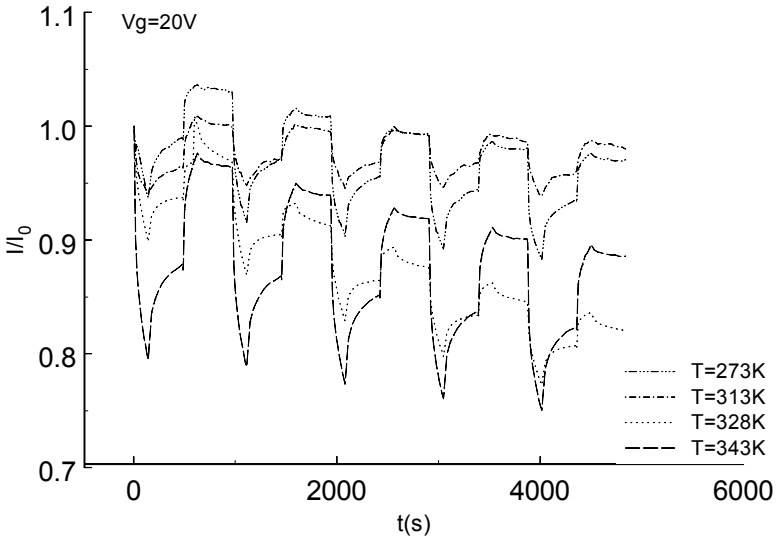

Fig. 6.19. Tests performed at the same gate bias (V_g = 20 V) and different temperatures using DUT 3 TFTs.

Calculating the dispersion coefficient in S+ for each applied stress and temperature, it appears that α increases with temperature and applied voltage stress (fig. 6.20).

The dispersion coefficient versus temperature is shown in fig. 6.21. For T < 343 K, the coefficient α has a linear dependence with applied stress

temperature fitted by equation: $\alpha = kT/kT_0 + \alpha_0$ where $T_0 \approx 200$ K and $\alpha_0 \approx -1.29$ and this is in contrast to the relation $\alpha = kT/kT_0$ with $T_0 = 500 - 700$ K as reported by many papers. The difference in the reported T_0 is discussed in chapter 4. For DUT 1 the fitting parameters are $\alpha_0 = -0.98$ and $T_0 = 250$ K and for DUT 2 they are $\alpha_0 = -0.76$ and $T_0 = 294$ K. The values of the characteristic temperatures T_0 are similar to the ones Libsch found and resemble the slope of conduction band tail as obtained from time-of-flight measurements mentioned in chapter 2. Non-zero α_0 and T_0 in the range $200 - 300$ K support the idea of a multi-trapping motion of the carriers at the interface instead in the bulk of a-Si:H [4, 33]. For $T > 343$ K, it is believed that α becomes temperature independent [33].

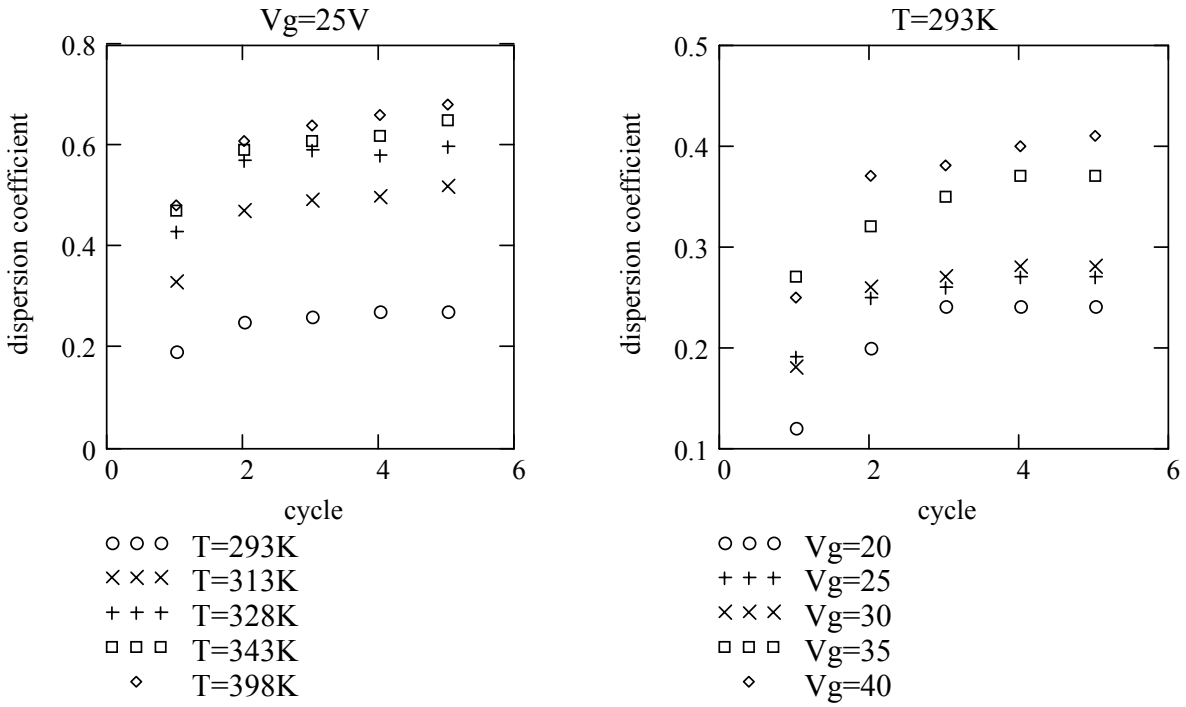

Fig. 6.20. Temperature dependency of the dispersion coefficient α in S+ of each stress cycle at $V_g = 25$ V (left). Bias stress dependency of the dispersion coefficient α in S+ of each stress cycle at $T = 293$ K (right).

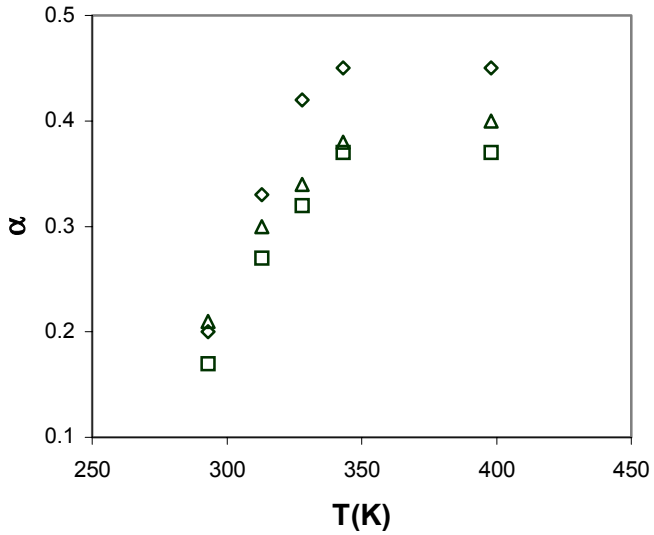

Fig. 6.21. α in S+ of the first cycle for three DUT (DUT 1 - triangles; DUT 2 - circles; DUT 3 - squares) versus temperature at $V_g = 25$ V bias stress

6.6. Conclusion

A new experimental technique and a model were used to explain the cause of drain current (I_{sd}) degradation in a-Si:H/SiN TFTs at room temperature and low gate voltage stresses.

The method of measuring I_{sd} is flexible and allows changes in the sequence of the applied bias stress and in the duration of each stress/relaxation period. By alternating the stress and relaxation, the device is progressively degrading. The short and long time degradation can be described in a single test: stressing and relaxing the device in one cycle with four sequences and repeating the cycle for many times.

A Progressive Degradation Model, PDM, which makes use of charge trapping and of defect creation theory is proposed to explain the experimental data. Alternating periods of stress and relaxation are described by a continuous function involving two parameters namely an interface charged traps density, D_{int} and a dispersion coefficient, α. PDM achieves a consistent fit under any bias condition and ambient temperature showing that the degradation can be modelled quantitatively yielding the number of traps involved, their position and

the charge dispersion coefficient. It has been shown that this model rather than other models in the literature best describes the drain current transient that occurs during the entire sequence of biases.

The results of testing drain current in a-Si:H/SiN TFTs show that the degradation is due to a combined effect of charge trapping at the interface (a few atomic layers from the crystallographic interface) and interfacial defect creation.

Experiments performed on N-rich and Si-rich SiN show that the stoichiometry of the gate insulator influences the devices reliability in terms of current values. The degradation of the drain current is more severe in the devices with Si-rich (sub-stoichiometric SiN) than in N-rich SiN (above-stoichiometric SiN). In terms of PDM, lower D_{int} and α are obtained for devices with N-rich SiN than for devices with Si-rich SiN.

It has been proven that the application of a negative stressing period at the beginning of a TFT duty cycle improves the stability of the device reducing the decay of the drain current during the following positive stressing period. Firstly applied negative stressing plays the role of an 'annealing' to a-Si:H/SiN TFTs whereas the positive stressing does the same for a-Si:H/SiO_2 TFTs. The severe current degradation that appears in a-Si:H/SiN TFTs in the first period of applied positive gate voltage stress is reduced with 20 % if prior to the stressing cycle the device is subjected to a period of negative stressing followed by relaxation.

A comparison between a-Si:H/SiN and a-Si:H/SiO_2 TFTs have pointed out that positive bias causes the strongest degradation of I_{sd} in a-Si:H/SiN whereas negative bias causes the strongest degradation of I_{sd} in a-Si:H/SiO_2 devices. In the light of the defect pool model, a different type of interface between a-Si:H and these two insulators is a possible explanation for this different behaviour.

As explained in chapters 4 and 5, the defect pool model does not state exactly where the ambipolar defects are created: at the interface with the insulator and/or in the semiconductor bulk. It only assumes that the creation/removal of defects at room temperature is very slow. The measurements performed in this chapter show that the first applied period of gate voltage stress (with positive polarity in devices with SiN as gate insulator and negative polarity in devices with SiO_2 as gate insulator, respectively) causes a fast and severe degradation of the drain current. This fast decay indicates that, at least at the beginning of stressing, the defects are created at the interface and not in a-Si:H bulk.

Appendix

Parameters of the models used for fitting in fig. 6.9.

negative stress

Dispersive charge injection model	Stretched exponential relaxation
$V_g^* = 19.2$ V	$V_0 = 17$ V
$\tau = 1 \cdot 10^6$ s	$\tau = 3 \cdot 10^8$ s
$\alpha = 0.26$	$\alpha = 0.31$

positive stress

Dispersive charge injection model	Stretched exponential relaxation
$V_g^* = 19.2$ V	$V_0 = 17$ V
$\tau = 4 \cdot 10^7$ s	$\tau = 7 \cdot 10^9$ s
$\alpha = 0.29$	$\alpha = 0.2$

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CHAPTER 7

CHARACTERIZATION OF INTERFACE TRAPS

This chapter presents the results of investigations regarding the density of interface traps, the energy of the traps and the location of the traps in a-Si:H and SiN.

Two techniques: QDLTS (Charge Deep Level Transient Spectroscopy) and STP (Slow Trap Profiling) were used. QDLTS is suitable for determining defect-related energy levels in the band gap of a-Si:H. STP is used to characterize the profile of slow traps close to the interface in a-SiN:H.

7.1. Introduction to Deep Level Transient Spectroscopy

The well-established techniques to study the semiconductor/insulator interface states are: comparative low-frequency (quasi-static) and high-frequency C–V measurement, small-signal admittance (conductance and capacitance) and the deep-level transient spectroscopy (DLTS) [1]. An exhaustive review of these techniques can be found in ref. [2] and comparative studies in ref. [3, 4]. The conventional DLTS, called capacitance DLTS, CDLTS, based on monitoring the gate-capacitance transients, has been proposed by Lang [5]. The technique had been adapted to MOSFETs by Wang [6].

Chen shows in ref. [7] that DLTS can be a powerful method of trap characterization not only for characterizing bulk traps in crystalline semiconductors but also for doped amorphous semiconductors. The method detects trap concentration about 10^{-4} times the concentration of shallow impurities in semiconductor [8]. The original capacitance DLTS failed for undoped a-Si:H and other high resistivity semiconductors, because a low frequency measurement is needed to make the dielectric response turn-on temperature low enough to observe the gap states over an appreciable fraction of the gap. A variant of DLTS called QDLTS or QTS has been proposed to study the traps in undoped amorphous semiconductors. It has been proven that QDLTS offers a unique capability to deal with dielectrics and high-resistivity materials where the carrier concentration is about or smaller than 10^{12} cm^{-3} [9, 10]. In fact, QDLTS technique followed a suggestion of Winer [11]. The idea of

this experiment is to shift the Fermi level of an equilibrated a-Si:H film in a metal-insulator-amorphous semiconductor, MIAS by applying a bias voltage, and to monitor the resulting change in the defect distribution as the film re-equilibrates. The defect distribution is based on the defect-pool model that was described in previous chapters 2-4. According to the defect-pool model, the defect chemical potential depends on the Fermi energy and a shift of the Fermi level at the equilibration temperature should change the proportions among the densities of D^+, D^0, and D^- charged defects. The defects are 'active' (i.e. change the spectral distribution) at a certain temperature above equilibration. This is why, in QDLTS, the emitted charge function of time is recorded in spectra of temperatures. In these spectra, a peak corresponds to a trap level active at that temperature. The height of the peak is proportional to the trap density and the position on the temperature axis leads to the determination of the fundamental parameters governing thermal emission and capture: activation energy and cross section [12, 13]. QDLTS, the way in which it works and parameter calculation is presented in section 7.1.1. The experimental results are presented in section 7.1.2.

7.1.1. Basics of DLTS

For DLTS either a Schottky diode or a metal-insulator (generally oxide) - semiconductor is generally used. A MIAS device can also be used for the characterization of traps by QDLTS, but in this case the insulator has to be thin and can be made in intimate contact with the semiconductor [14].

The method is based on measurement of the charge transient response of a MOS or diode-like structure under periodically applied voltage steps to the gate electrode. The device, most commonly a Schottky diode, is reverse biased with a trap filling pulse. The trap filling pulse will establish the saturation of trap occupancy. At the end of the pulse, the sample is heated at a constant rate and the current associated with thermal emission of trapped carriers flows in the external circuit until the trap occupancy is restored to its steady state (fig. 7.1) [15].

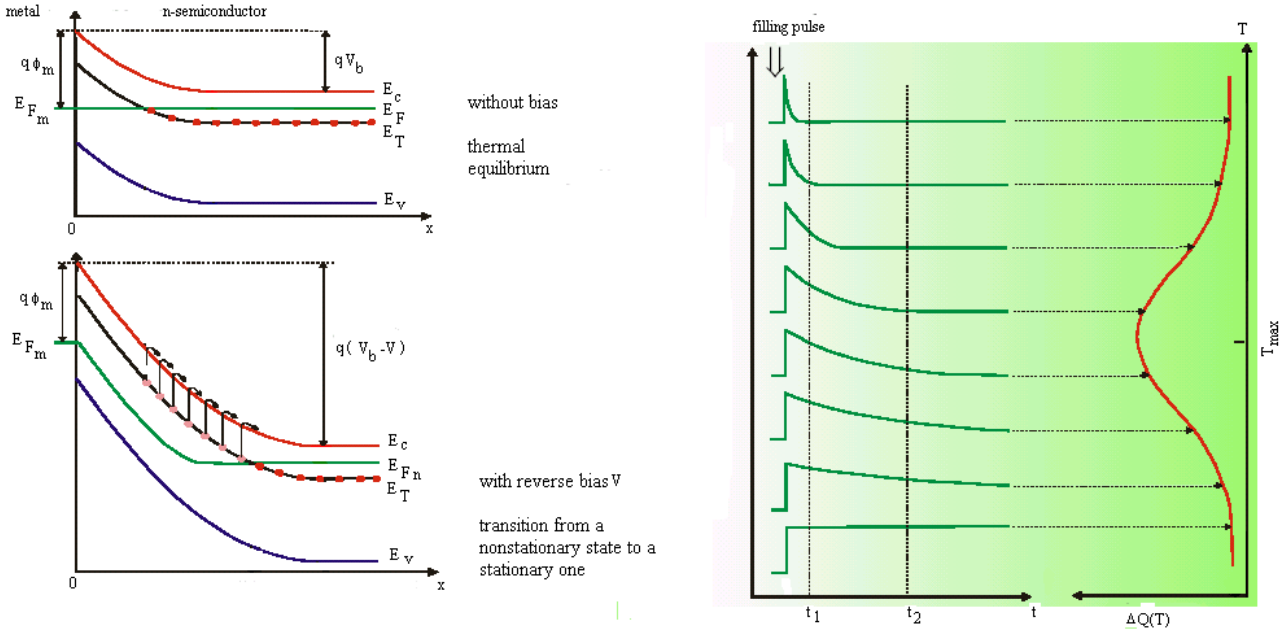

Fig. 7.1. Band diagrams of an n-type Schottky diode during transient spectroscopy and the corresponding DLTS spectra of temperatures, source: http://sesam.desy.de/talks/Ioana-Brainstorm9thJan2003.pdf

The thermally induced emission of the carriers (in this case electrons) occurs with an emission rate defined as $e_n = \frac{1}{\tau} = N_c \cdot \sigma \cdot v_t \cdot \exp\left(-\frac{E_c - E_t}{k \cdot T}\right) \propto \sigma \cdot T^2 \cdot \exp\left(-\frac{E_a}{k \cdot T}\right)$ where N_c is the effective density of states in the conduction band; σ - capture cross section; v_t - thermal velocity of carriers; $E_c - E_t = E_a$ is the trap depth below conduction band; k - Boltzmann constant and T is temperature [16]. Quantity $\nu = N_c \cdot \sigma \cdot v_t$ is the attempt-to-escape frequency.

During relaxation process toward steady state (interface traps emit their charge), a current transient (for uniform trap distribution) is recorded as $I(t) = A \cdot q \cdot N_t \cdot \frac{\exp\left(-\frac{t}{\tau}\right)}{2 \cdot \tau}$ where A is sample area, q elementary charge, N_t - trap density in semiconductor and τ is a relaxation time of the carriers.

The current transient is related to the charge emitted in time as $Q(t)=\int_0^t I(t`)dt`=\frac{A\cdot q\cdot N_t\cdot\left(1-\exp\left(-\frac{t}{\tau}\right)\right)}{2}$ and hence to the density of traps.

The charge transient is measured at two time instances t_2 and t_1 as the temperature is varied. The measured value of the QDLTS signal at a temperature T is the charge difference $\Delta Q(T)=Q(t_1)-Q(t_2)$

The explicit form of the time and temperature dependence of the signal is: $\Delta Q(t)=Q_0\cdot\left(\exp\left(\frac{-t_1}{\tau}\right)-\exp\left(\frac{-t_2}{\tau}\right)\right)$; where τ is the time constant of the relaxation that is temperature dependent and Q_0 is a proportionality constant that incorporates the density of traps.

At a certain temperature (T_{max}) that represents the temperature at which the trap emits the carriers, ΔQ shows a maximum (peak) corresponding to the maximum of the emission. The condition of maximum signal is obtained by differentiating ΔQ with respect to τ. The peak ΔQ_{max} at T_{max} is obtained at $\tau_{max}=\frac{t_2-t_1}{\ln\left(\frac{t_2}{t_1}\right)}$ that represents the maximum of carrier emission from traps and defines the 'rate-window', RW as τ_{max} = 1/RW. The rate-window is nothing more than a filtering operation since only traps with time constants ~ 1/RW are measured.

The trap activation energy is obtained from a graph $\ln(\tau_{max})$ or $\ln(RW)$ versus $1/T_{max}$ and the density of traps is determined from the height of ΔQ at T_{max} as $N_t=\frac{\Delta Q(T_{max})}{A\cdot q\cdot\left(1-\exp\left(-\frac{t_1}{\tau_{max}}\right)\right)}$.

7.1.2. Results of QDLTS

In this section, the results obtained using QDLTS are presented; traps are identified and the activation energy of the trap is calculated.

QDLTS measurements were conducted on especially made MIAS structures Al/a-Si:H/a-SiN_x:H/c-Si(n^+); where the thickness of the a-Si:H and a-SiN_x:H layers being 1000 nm and 10 nm, respectively. The gate potential V_g is defined as that of the c-Si(n^+) electrode against the top Al. The area is 10^{-6} cm^2. The a-Si:H and SiN films are PECVD deposited according to the recipe described in chapter 3 and corresponding to a-Si:H 1 and SiN 3 films (table 3.1).

By means of QDLTS, the charge transients were measured over a temperature range from 100 K to 470 K swept at a rate of 10 K/min and at different rate windows RW ranging from 100 to 2000 s^{-1}. The applied bias voltage was –1.5 V and excitation pulse 3 V.

The QDLTS spectrum on the samples described above is reproduced in fig. 7.2. The a-Si:H traps responded only at 100, 200 and 400 s^{-1} whereas no activity has been detected at higher RW in the chosen domain of temperatures. The sampling times were t_1 = 7 ms and t_2 = 14 ms for RW = 100 s^{-1} and two peaks had been observed: one at 400 K and another at 440 K. For RW = 200 s^{-1} and 400 s^{-1} only one peak at 400 K is observed.

One notices that, by decreasing RW, the peak at 400 K decreases and at the lowest RW it remains just a 'tail' in comparison with a new peak that appears at 440 K and dominates.

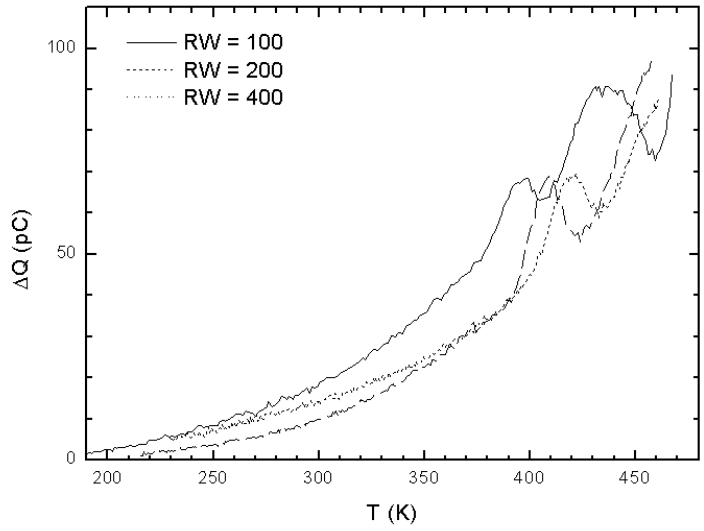

Fig. 7.2. The QDLTS spectra of the MIS capacitor at different rate windows.

The signal that peaks at $400\ \mathrm{K}$ for $\mathrm{RW} = 200$ and $400\ \mathrm{s}^{-1}$ has been found to be about $25\ \mathrm{pC}$ high. The maximum width of trap distribution (from the half width of the peak) is $\Delta E = 0.1\ \mathrm{eV}$, indicating a narrow distribution.

The density of the traps that are active at $T_{max}= 400\ \mathrm{K}$ is calculated using a simplified formula referenced in [17]:

$N_t \sim \dfrac{\Delta Q(T_{max})}{A \cdot q \cdot \Delta\Phi \cdot f(t_1, T_{max})} = 10^{13}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$; where $\Delta Q(T_{max}) \sim 25\ \mathrm{pC}$ is the peak height; $A = 10^{-6}\ \mathrm{cm}^2$; $\Delta\Phi = 0.1\,\mathrm{V}$ is the drop of the surface potential and $f(t_1, T_{max}) = 1 - \exp\left(-\dfrac{t_1}{\tau_{max}}\right) = 0.17$.

The activation energy is obtained from the slope of the graph $\ln(\mathrm{RW})$ versus T_{max} and the trap capture cross section from the intercept [17] (fig. 7.3). It was found that the activation energy is $E_a \sim 0.9\ \mathrm{eV}$.

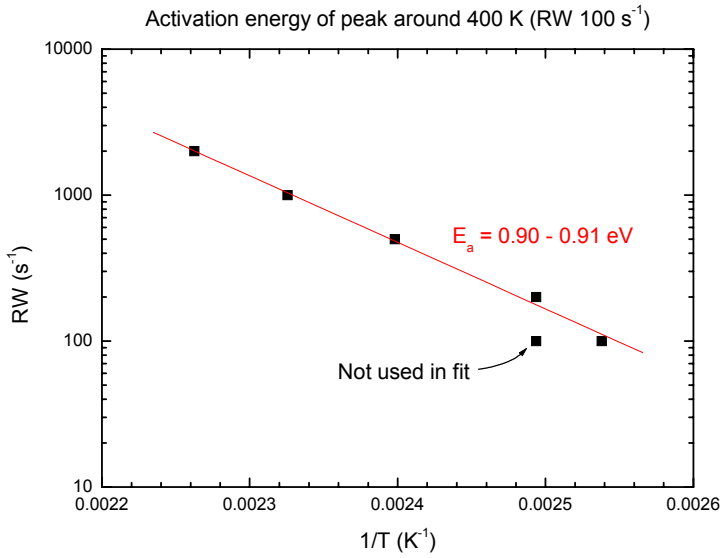

Fig. 7.3. Rate window as a function of temperature

The active trap at 400 K appears to be located around equilibrium Fermi level at 0.9 eV. The trap that gives a peak in QDLTS signal at 440 K has emission times much larger than the rate window of the experiment.

The activation energy of the trap at 440 K (RW = 100 s^{-1}) could not be deduced from the experiment but, most probable, it is a trap related to negative charge defects that are found in the literature to lay at 1.3 eV below the conduction band of a-Si:H [18-22]. The QDLTS measurements performed by different groups on undoped a-Si:H determined three groups of traps, with activation energies of 0.63, 0.82, and 1.25 eV, in a good agreement with the existence of the D^+, D^0, and D^- dangling bond states, predicted by the defect-pool model [22-25].

The presence of active defects above 400 K has been confirmed by high-frequency C–V measurements at this elevated temperature on the same sample as described in 7.1.2. The interface traps do not follow the high frequency signal and total capacitance is due to contributions from the gate insulator and semiconductor bulk.

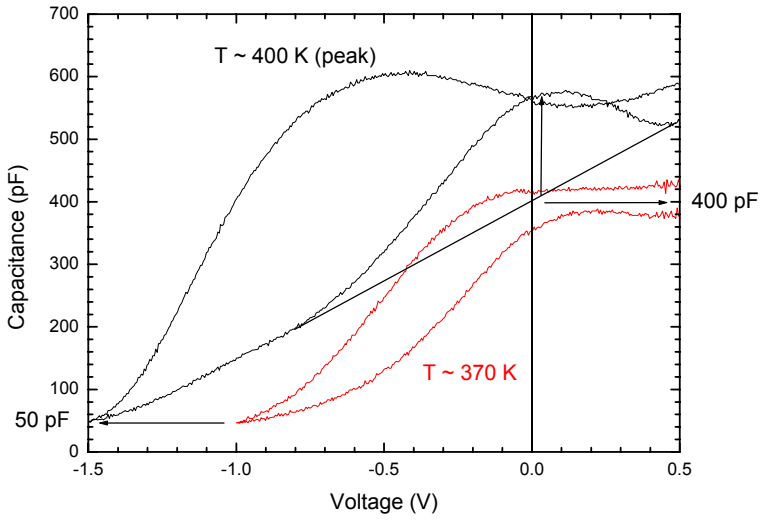

Fig. 7.4. High frequency C–V curves at different temperatures. The 'hump' of the curves about 400 K indicates the presence of active interface traps whereas below 400 K the curves run smoothly. Lines and arrows were use to identify the position of the hump in respect to the gate voltage and to estimate the value of the capacitance without the hump.

As it can be seen in fig. 7.4, above 400 K a 'hump' in the curve indicate the presence of an active trap in a-Si:H bulk. The hump reaches maximum at about 0 V gate voltage and the capacitance without the peak is about 500 pF. At 370 K, where the traps behave as frozen, there is no peak and the capacitance is about 400 pF.

7.2. Introduction to Slow Trap Profiling

Relaxation of the drain current of transistors reported after an electrical degradation stress was explained by the presence of slow traps near the semiconductor interface in the gate insulator [26]. These traps are not 'true' interface traps because the reported characteristic time constants of interface traps are shorter than a tenth of a second [27]. This additional type of state, termed slow charging states or border traps [28], was concluded also from experiments showing slow relaxation of the flat-band voltage on the time scale

of minutes up to hours after removing the stress voltage [29]. The transition of channel mobile carriers to and from slow traps occurs by direct tunnelling between the silicon band edges and insulator traps [30].

Usually, the density of slow traps had been observed in MOS capacitors from variations of the flat-band or midgap voltage as measured by conventional high-frequency C–V methods. Consequently, only the charging state at flat-band conditions is attained. An estimation of the total amount of traps being charged/discharged during the C–V sweep or a spectral resolution of traps as a function of interface potential is not attained by conventional methods.

In the STP technique, by monitoring of the gate charging currents as a function of time, it is possible to identify charging of slow traps in the gate insulator. The software controlled experimental set-up implicitly defines 'slow traps' as border traps in the insulator and discriminates them from fast interface traps via the time resolution (time elapsing from the gate-bias step to the first reading) and from fixed oxide charges via the current resolution of the overall experimental set-up.

STP includes two functions: first a quasistatic C–V measurement and second a measurement of the charging current. A complete study of STP method for Si/SiO_2 capacitors is referenced in [31]. To our knowledge this is the first time that STP is applied to a-Si:H/SiN structures. The way in which STP works is presented in section 7.2.1 and the results of the experiments are presented in 7.2.2 and 7.2.3.

7.2.1. Basics of STP

First, a quasistatic C–V measurement is performed. The voltage is ramped in a staircase fashion. The current at the gate, through the capacitor, is measured at a delay time after each voltage step. A flash of light is applied at the onset of the stepping in order to ensure that the structure is in thermal equilibrium. From the C–V curve, the band bending that relates directly the measured states to their position in the band gap is deduced.

In fig. 7.5A, the energy band diagrams of a (n type) MOS biased from accumulation towards inversion are depicted. In the same picture the quasistatic and the current-voltage curves are shown from accumulation towards inversion. In accumulation (a) the electrons flow from the surface towards the bulk of a-Si:H. Voltage stepping produces spikes of current. In depletion, the a-Si:H

surface is depleted of electrons. As weak inversion approaches (b), the capacitance increases slowly and a 'glitch' in current appears due to the contribution of slow states located around and below Fermi level (arrow 2). In strong inversion, the voltage stepping technique does not produce any spikes in current. The slow states are above Fermi level and hole generation from the valence band dominates (arrow 1). In fact there are two glitches of the current: one appearing above flatband and the other one below flatband (fig. 7.5B). The nature of the glitch above flatband is possibly due to interface traps and it was filtered out.

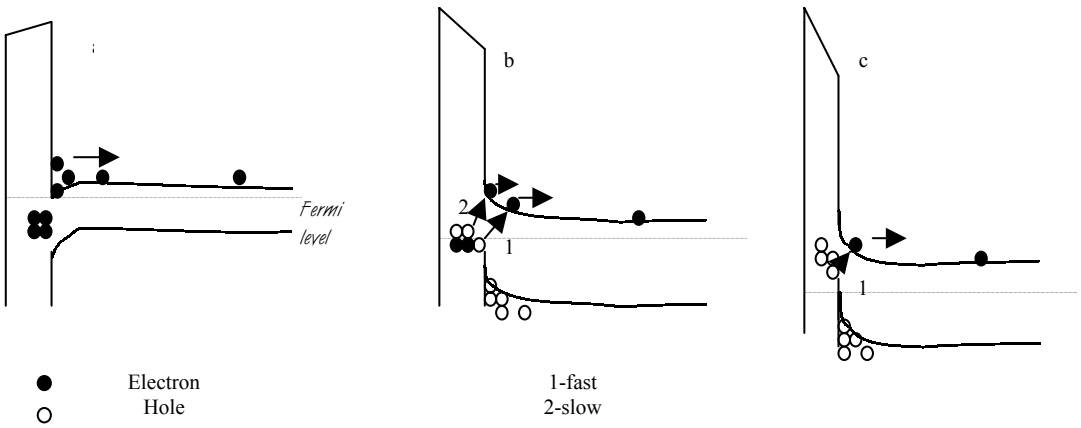

Fig. 7.5A.. Sketch of n-MOS energy band diagrams at 3 points (a, b, c) corresponding to the movement of electrons and holes in accumulation, depletion (weak inversion) and inversion.

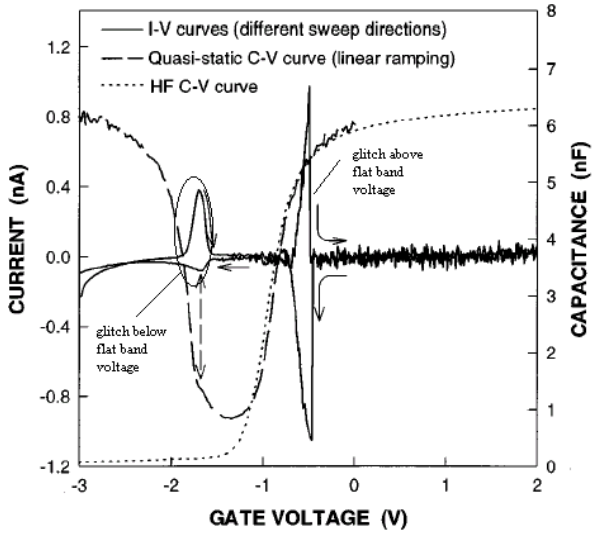

Fig. 7.5B. C–V and I–V measurements performed by STP on MOS capacitor showing the glitches in current below and above flat band voltage (arrows show direction of sweeping) [32]

The current glitch below flatband is emphasized in the following according to the experimental evidence provided in ref. [32].

Tanner, Dimitrijev and Yao studied the influence of current stress, repetitive stepping, oxide thickness and temperature stress on the magnitude and position of the glitch. They noticed an increase of the magnitude of the current glitch after current stress and explained it as traps generation in the oxide and at the interface with semiconductor, while the relative thickness independence of the glitch had been interpreted as an indication that the traps are near the oxide-semiconductor interface. The reduction of the current when the measurement temperature is lowered indicates that the tunnelling current is reduced, which is consistent with the tunnelling theory described in this thesis in chapter 6.

The current is a function of response time and applied step voltage and the bias voltage. Dividing the current by sample area, electron charge and voltage step it gives the value of interface trap density per unit area. The result is a three dimensional representation of the slow traps density as a function of the applied voltages and the response time of the traps. The time response of the trap is proportional to trap distance from the interface.

The measured charge, q_m, for each gate voltage and time is converted to the interface state density $[cm^{-2}V^{-1}s^{-1}]$ by: $D_{it} = \frac{q_m}{e \cdot \Delta V \cdot \Delta t \cdot A}$; where Δt is the stepping time (time between two measurements), ΔV is the stepping voltage, A is capacitor area.

The method of investigation becomes more meaningful when the gate voltage is converted to band bending Fermi level at surface as it will be shown later on in this chapter. In this case, the gate voltage at which the trap is active corresponds to an energy $E_f - E_{mg}$ where E_{mg} is mid-gap energy and E_f is the Fermi level corresponding to gate voltage [32].

It is possible to determine the energy position of the traps located at the interface insulator/semiconductor in the insulator, their density, the time-response and the distance of the traps from the interface from the tunnelling model [33].

7.2.2. Results of STP

The measurements were conducted on structures Al/a-Si:H/a-SiN:H/c-Si, the thickness of the a-Si:H and a-SiN:H layers were 250 nm and 300 nm,

respectively. The samples used are MIAS capacitors deposited on the same wafer with a-Si:H/SiN TFTs labelled in chapter 3 as TFT 3 and 4. Capacitor area was $A = 0.026\ cm^2$. For each measurement, a fresh device was used.

First, quasistatic C-V measurements have been performed. The voltage step size used in this experiment was either 10 mV or 20 mV. The gate voltage range than can be obtained with the equipment is between –10 and 10 V. This range of voltages limits somehow the probing of the entire band gap of a-Si:H as it will be shown later in this section.

The time step size consists of two parts; delay time that is set by user to 10 ms, and a measurement time whose minimum value is 6.5 ms. There is also the possibility to hold a stress voltage applied to the sample for a set time before the stepping starts. This time is called holding time but in these experiments holding time was 0 s.

The measurements have been performed at room temperature.

The profile of slow traps of a fresh device is illustrated in fig. 7.6.

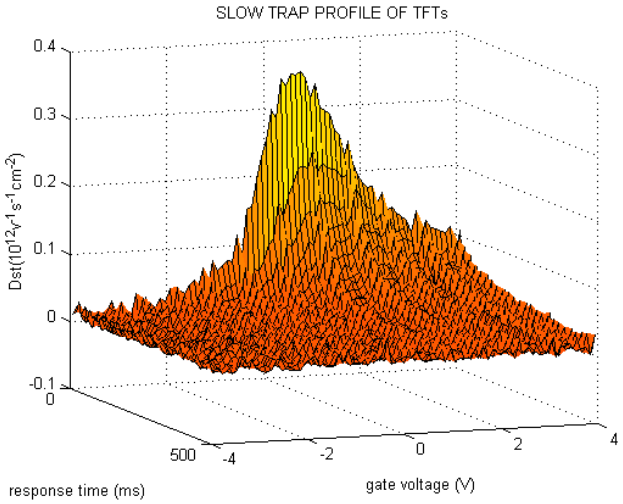

Fig. 7.6. Slow trap profile of MIAS ($A = 0.025\ cm^2$, $\Delta t = 50$ ms, $\Delta V = 0.2$V). A positive bias on gate prior to measurements will shift the peak to the right whereas negative bias will shift the peak to the left.

The main peak corresponds to border traps with response between 10 ms to 100 ms and the low level plateau to the right of the peak is due to 'true' insulator traps, with response time between 100 ms to 500 ms situated at some distance from the interface.

The peak shifts very slowly towards negative voltages under negative stress and it shifts towards positive voltages under positive stress (fig. 7.7 and 7.8).

The density of traps does not show any significant increase of the traps when the device is subjected to –10 V for 8 h. The density almost doubles when subjecting the devices to –10 V for 12 h and the profile shows a clear peak that appears at the minimum of the voltage range.

The density of border traps does not appear to increase noticeably after subjecting the device to 10 V of gate bias stress for 8 h. The density increases noticeably when subjecting the devices to 10 V for 24 h. The profile shows no clear peak but a wide peak with ten times higher density of traps than in the fresh device. This result indicates a deteriorated device due to stress.

The results of positive and negative stressing indicate the existence of border traps that exchange charge with a-Si:H channel during gate stress. In order to see the energy of the border traps, the gate voltage is going to be converted to band bending in sub-section 7.2.3.

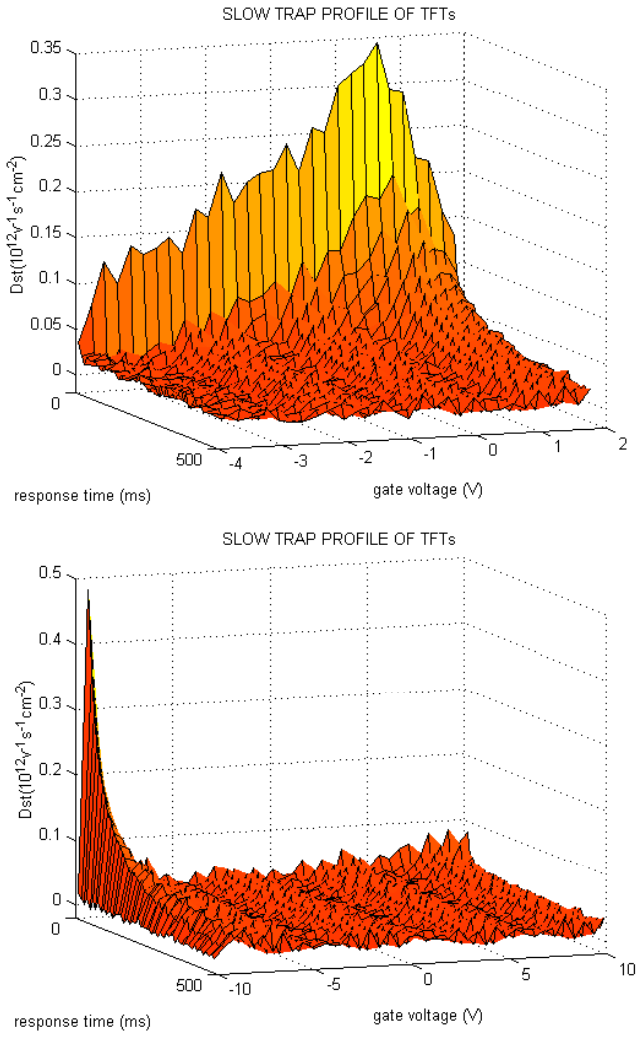

Fig. 7.7. Slow trap profile of a device subjected to –10 V, 8 h and 12 h of stress (down)

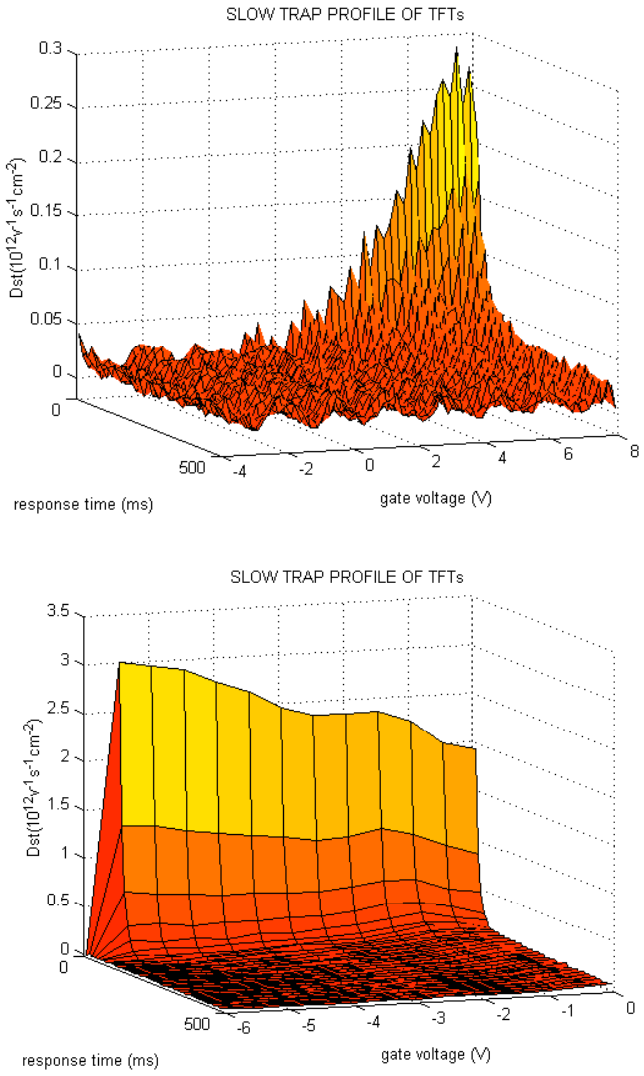

Fig. 7.8. Slow trap profile of a device subjected to +10 V for 8 h and 24 h of stress.

7.2.3. Band bending calculation

The dependence of the band bending on the applied gate voltage is to be derived in the following for the STP measurements presented in this chapter.

The correspondence between the energy range probed by measurement and the gate voltage swept during the measurement was proposed by Berglund in formula [34]:

$$E - E_0 = q \cdot \left[\Psi(V_g) - \Psi(V_{g_0})\right] = \int_{V_{g0}}^{Vg} \left(1 - \frac{C_{LF}(V_g)}{C_i}\right) dV$$

where $E - E_0$ is the energy of the states probed at the gate voltage V_g corresponding to the band bending $\Psi(V_g)$; V_{g0} is an initial gate voltage corresponding to $\Psi(V_{g0})$ and E_0. C_{LF} is the quasistatic capacitance expressed by formula: $\frac{1}{C_{LF}} = \frac{1}{C_i} + \frac{1}{C_{bs} + C_{int}}$ that describes the MIAS capacitance as equivalent to an electrical circuit where C_i is the insulator capacitance, C_{bs} is the semiconductor bulk states capacitance and C_{int} is the interface states capacitance.

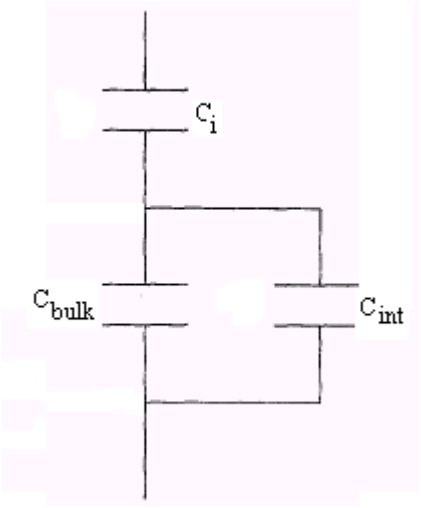

Fig. 7.9. Equivalent electrical circuit of the MIAS structure in quasistatic regime, showing the contribution of interface traps, bulk states, (free carriers capacitance is neglected) to the total capacitance.

When C–V is done on MIS structures (with thermally grown oxide as insulator), the contribution from charge injection in gate insulator and bulk states is usually neglected due to large time constant and only contribution to C_{LF} due to interface states is considered dominant. When an amorphous insulator as silicon nitride is used instead of thermally grown oxide the situation complicates due to possible charge trapping in the insulator. The insulator leakage is frequently reported and many authors proposed to use MIAS with a very thin insulator [35].

Kleider and Dayoub have shown that in MIAS structures, the contribution of bulk states to total capacitance would be more important than the contribution from interface states [36]. In particular, the density of bulk states at a given energy is not simply related to the capacitance as in the crystalline semiconductor but also to the derivative and the integral of the capacitance with respect to and over the gate voltage, respectively. Moreover, the bulk a-Si:H states are proven to be not uniformly distributed in the whole semiconductor layer [37] and a non-homogeneous density of states has to be taken into account when calculating the bulk capacitance as extensively shown in ref. [38]. According to ref. [38], the changes in DOS are reflected to the changes in C–V curves. However, when a measurement is performed at room temperature like in the case presented here, without re-equilibration of bulk DOS, the distribution of bulk defects can be considered frozen-in and DOS changes very slowly with the applied bias as mentioned in chapter 5. Then, the DOS revealed by C–V measurements will reflect DOS 'seen' by Fermi level at frozen-in.

The band bending as a function of bias is calculated here from the quasistatic C–V curve (fig. 7.10) by using Berglund's equation as described by Uren [39] and Kerber [40].

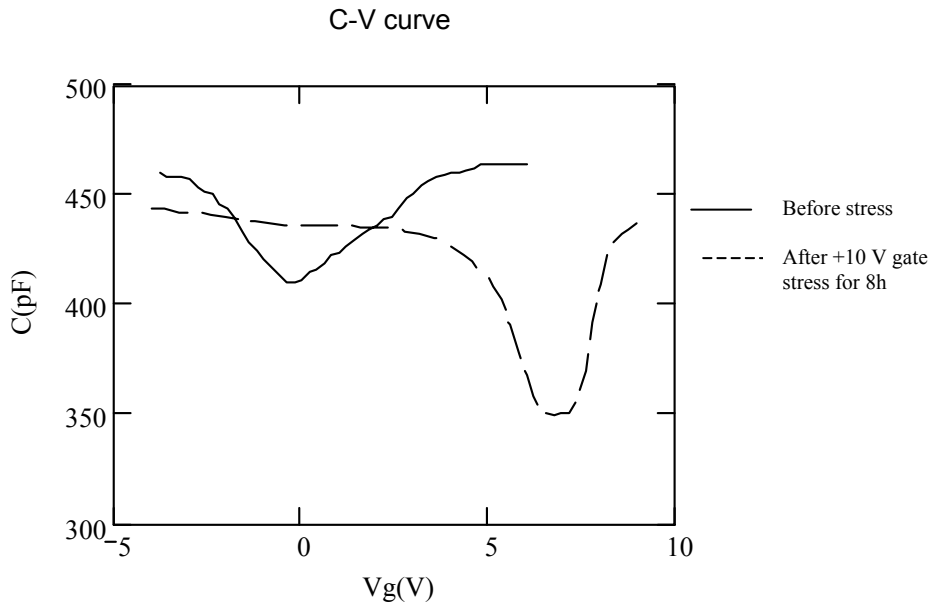

Fig. 7.10. Quasistatic C–V curves of MIAS capacitor

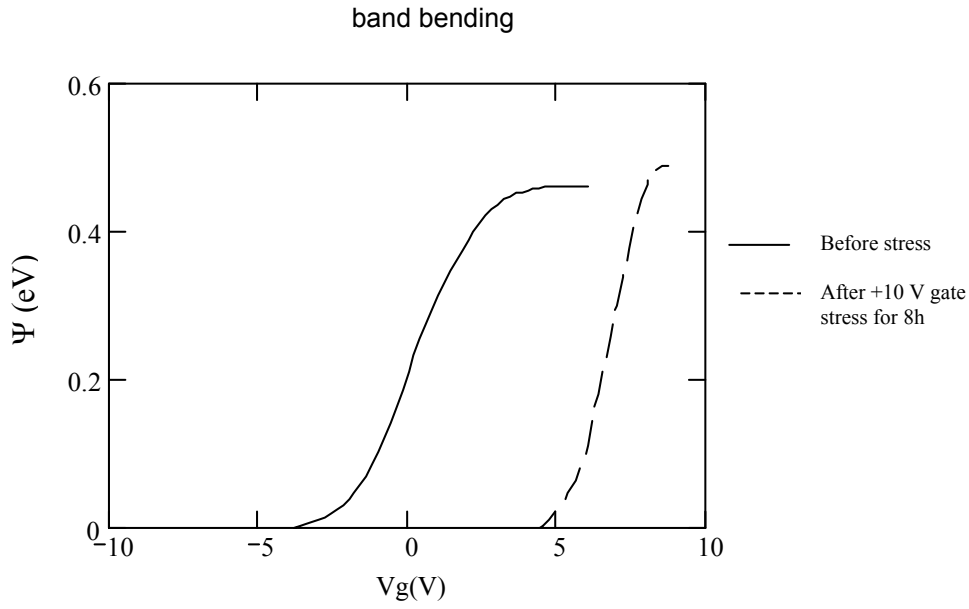

Fig. 7.11. Calculated band bending of the MIAS presented in fig. 7.10.

The dependence of the low frequency capacitance on the gate bias is known from C–V data presented in fig. 7.10. Integrating Berglund's equation, the dependence of the band bending with the gate voltage is obtained (fig. 7.11). The integral has been solved numerical by using MathCAD.

As it can be seen in fig. 7.11, the energy of the traps probed by STP ranges from 0.4 to 0.5 eV above valence band corresponding to gate voltages from ranging from –10 to 10 V. According to Kleider, the states probed in this short range of gate voltages corresponds to a local minimum of DOS at the intercept between the DB states distribution and the valence band tail. These traps might be due to stressed Si-Si bonds that resulted because of lattice mismatch between a-Si:H and SiN.

7.3. Conclusion

A characterization of fast and slow traps in a-Si:H and SiN close to the interface has been performed by means of QDLTS and STP.

A trap signature with activation energy of 0.9 eV (below conduction band) was identified in QDLTS measurements as neutral defect state in a-Si:H. The defects appear to be active above 400 K. The deep defects in a-Si:H are not active at room temperature so that the defect creation in a-Si:H bulk cannot be related to the charge transients described in chapter 6.

Traps with slow response time had been found by performing STP measurements to lay in SiN at the interface. These traps exchange charge with a-Si:H channel when a gate voltage stress is applied. The traps appear to correspond to a local minimum of a frozen DOS at the valence band tail.

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ANNEXE

EXPERIMENTAL TECHNIQUES

This annexe describes the measurement techniques that have been used in this thesis for thin film characterization, device characterization and trap characterization. Thin film characterization section describes the techniques used for characterization of as-deposited amorphous silicon and silicon nitride layers. The device characterization section describes the techniques used to characterize the thin film transistors. The trap characterization section describes the techniques used to characterize the traps located in the amorphous silicon bulk and at the interface with silicon nitride. Thin film characterization is presented in section A.1, device characterization in section A.2 and trap characterization in A.3.

A.1. Thin film characterization

The atomic composition of a-Si:H and a-SiN:H has been determined using Fourier Transform InfraRed spectroscopy (FTIR) and Rutherford BackScattering (RBS) measurements. FTIR is also used for characterisation of the interface between a-Si: H and a-SiN. FTIR and RBS are described in sections A.1.1 and in A.2.1, respectively.

The degree of amorphization of a-Si: H has been probed by X-ray diffraction (XRD) that is described in section A.1.3.

A.1.1. Fourier Transform InfraRed Spectroscopy

Infrared Spectroscopy is a measurement technique whereby spectra of materials are collected based on the response from a pulse of electromagnetic radiation.

Instead of varying the energy or wavelength of the electromagnetic radiation and plotting the response (usually the intensity of transmitted radiation) as a function of radiation energy (or frequency), Fourier Transform Spectroscopy, FTIR, exposes the sample to a single pulse of radiation and measures the response. It is used in this thesis to reveal information about atomic structure (atoms' bonding) of a-Si:H, SiN and interface between them

and to calculate the amount of H in a-Si:H. The samples were a-Si:H and SiN films with $1\ \mu m$ thickness deposited on highly resistive Si wafers.

FTIR spectrum is recorded as the absorbance in the sample versus the wavelength of the radiation. The sample for analysis is compared with a background spectrum that is the spectrum of a bare Si wafer.

The FTIR spectrum of a-Si:H and SiN exhibits a number of absorption peaks corresponding to bonding arrangements (rocking and stretching Si-H bonds) within the molecule of a-Si:H and SiN. FTIR of the a-Si:H/SiN interface revealed bonding arrangements at the interface a-Si:H/SiN. Comparing FTIR of the interface with FTIR of bare Si wafer a convention had been made: upside peaks are vibration modes in SiN and downside peaks are vibration modes in a-Si:H and interface.

The integrated absorption α of a peak corresponding to the wavelength λ is calculated as $I = \int \frac{\alpha(\lambda)}{\lambda} d\lambda$.

The FTIR is used also to calculate the percentage of bonded H in a-Si:H. The hydrogen in a-Si:H is exclusively bonded to Si-H rocking and stretching vibration modes that appear at $\lambda = 630$ and $2000\ cm^{-1}$ [1]. The density of H in a-Si:H (n_H) is proportional to the integrated absorption of peaks at 630 and $2000\ cm^{-1}$ and it is calculated as $n_H = A \cdot I$ where A is a proportionality factor. The proportionality factor used in evaluating the H content of our films is $2.1 \cdot 10^{19}\ cm^{-2}$ and $9 \cdot 10^{19}\ cm^{-2}$ respectively.

The H content in SiN is evaluated by integrating the peaks corresponding to Si-H at 2200 and N-H at $3300\ cm^{-1}$ using proportionality factors of $2.8 \cdot 10^{20}$ and $1.4 \cdot 10^{20}\ cm^{-2}$ respectively [2].

The measurements of a-Si:H and SiN are presented in chapter 2. The FTIR measurements of a-Si:H/SiN interface are shown in chapter 3.

Equipment used: Biorad FTS-60A Spectrometer with λ in the range of $400 - 4000\ cm^{-1}$ and a resolution of $4\ cm^{-1}$.

A.1.2. Rutherford Backscattering

Rutherford Backscattering, RBS, is one of the most frequently used techniques for quantitative analysis of composition, thickness, and depth profiles of thin solid films. Details about this technique are referenced in [3, 4].

RBS is used in this thesis to measure the stoichiometry of SiN thin films as the ratio between nitrogen and silicon in silicon nitride.

The SiN target was bombarded with high-energy ions He^{2+}. These ions collide with atoms in the target. Upon elastic collisions of ions with the target nuclei, the ions backscatter and carry information about the atoms they backscattered from. A detector is placed under a fixed angle to collect the particles that scatter from the target. The probability of backscattering from different atoms in SiN is proportional to the square root of the atomic number thus allowing the determination of SiN composition.

The RBS spectrum is given in a plot of counts (intensity of the beam) versus energy. Peaks at characteristic energies identify the target elements. Dividing the area of regions 1 and 2 of simulated RBS spectra (fig. A.1) to experimental spectra, the ratio N/Si in SiN samples is deduced [5, 6]. The RBS measurements of SiN samples are discussed in chapter 2.

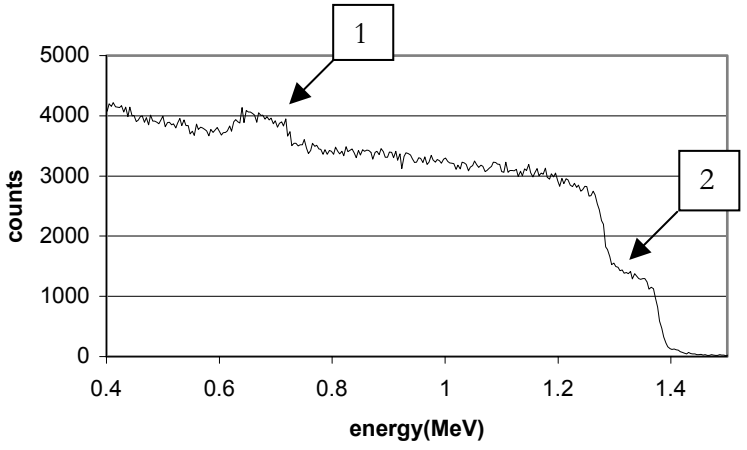

Fig. A.1. RBS spectra of a-Si: $H/SiN_{1.46}$ TFT. Legend:
1. He^{2+} backscattered from SiN; 2. He^{2+} ions backscattered from a-Si:H.

Equipment used: A van de Graaff accelerator.

A surface barrier detector under 165 degrees back reflection measures the scattered ions. By means of a multi channel analyser, the signal height that is proportional to the energy is converted into channels ranging from 0 to 2.4 MeV. For the calculation of compositions a special program provides a simulation, which gives an overall accuracy of 3 %.

A.1.3. XRD measurements

X-ray diffraction techniques give information about the arrangement of the atoms that compose a solid [7].

X-ray diffraction is used in this thesis to estimating the degree of amorphization of a-Si:H thin films.

X-rays are generated when a high energy beam of electrons strikes the a-Si:H target. In the target material, X-rays are scattered by variations in electron density. Where the electron clouds are ordered with respect to each other, the scattered X-rays interfere to produce a diffraction pattern characteristic of the ordering in the target.

If the a-Si:H target contains crystalline islands embedded in an amorphous lattice, a pattern due to a crystalline region and a pattern due to an amorphous material overlap with each other. The degree of crystallinity or the degree of amorphization is determined from a ratio between the area under the peak given by diffraction on a crystalline region and that of the amorphous material. Studies about the amorphization of a-Si:H are referenced in [8, 9]. The XRD spectrum of a-Si:H is presented in chapter 2.

Equipment used: X-ray diffractometer Philips Expert

A.2. Device characterization

The current-voltage (I–V) measurements are extremely important for TFT characterization. In this thesis, TFT electrical parameters such as mobility, threshold voltage and subthreshold slope are deduced from the drain current – gate voltage (I_d–V_g) measurements. From the drain current- drain voltage (I_d–V_d) measurements, information about the series resistance, current crowding is obtained. Moreover, the bias induced instabilities are usually investigated through changes of I_d–V_g characteristics of the TFTs.

The capacitance-voltage (C–V) measurements are useful for the extraction of other electrical parameters that cannot be deduced from the I–V measurements, for example the flat-band voltage. The bias induced instabilities are investigated through changes of C–V characteristics of the Metal-Insulator-Amorphous Silicon (MIAS) capacitors.

A.2.1. I-V measurements

The thin film transistor, TFT, is essentially applied as an electronic switch; when selected (on) it allows charge to flow through it and when off it acts as an barrier preventing or at least restricting the flow of charge. As mentioned in chapter 1, a TFT is a field-effect device. The gate can be considered the control electrode of the transistor; it turns the TFT on, partially on, or off. The source and drain are the entrance and exit, respectively, for charge to pass through the switch. In the case of a display, this is the charge that appears on the pixel. When a positive voltage V_g is placed on the gate, electrons begin to collect in the area above the gate, on the other side of the silicon nitride (gate insulator) in amorphous silicon. When the charge on the gate is increased to a certain point called threshold voltage, V_{th}, enough electrons have been attracted at the amorphous silicon surface to change the device from the non-conductive to conductive state; V_{th} marks the transition point between the two states. In other words, for $V_g > V_{th}$, a channel is build up at the amorphous silicon surface, i.e. the interface with silicon nitride. When the drain is biased positively with respect to source, the electrons flow from source to drain, through the channel, and a current, I_{ds} which magnitude depends on the applied gate voltage, is measured in the external circuit.

The above is only meant as a basic simplified description of a-Si: H/SiN TFT operation, the way in which I_{ds} depends on V_g and subthreshold swing, threshold voltage and mobility are deduced from this dependency is presented further on.

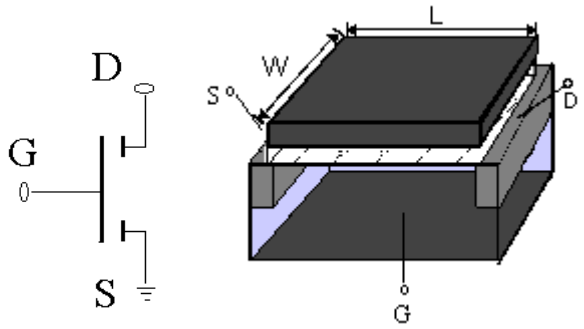

Fig. A.2. Gate, source and drain connexions for transfer characteristic I_d–V_g of our TFTs.

The characteristic I_d–V_g curves of TFT present three distinct regions of operation of the TFT: the subthreshold region, the linear region, and the saturation region. The connections of gate, source and drain are indicated in fig. A.2. The TFTs were a-Si:H/SiN TFTs with W/L = 2 (200/100, 120/60,40/20) or 5 (500/100, 300/60, 100/20). The thickness of a-Si:H and SiN were 250 nm and 300 nm, respectively.

In the subthreshold region, the gate voltage is lower than the threshold voltage and diffusion current resulting from the concentration gradient of electrons in the channel dominates the drain current. The subthreshold swing or subthreshold slope, S, is a parameter characteristic of the subthreshold region. By definition the subthreshold swing is given as: $S = \ln(10) \cdot \frac{dV_g}{d(\ln(I_{ds}))}$

The subthreshold swing has been calculated using MathCAD from the experimental data in the subthreshold region of I_d–V_g curves (where $V_g < V_{th}$) by using this formula.

If the drain voltage is very small comparing to the effective gate voltage (typically $V_d = 0.5$ V is used for the TFTs in this thesis), the channel region acts like a resistor and the drain current is dominated by drift; this region is called linear region. The drain current in linear region is usually expressed like in a MOSFET as: $I_d = \mu_{fe} C_{ins} \frac{W}{L}(V_g - V_{th})V_d$; where μ_{fe} is the field effect

mobility in the channel, C_{ins} is the insulator capacitance, V_g - gate voltage, V_d - drain voltage, W is channel width and L channel length as defined by the mask and V_{th} is the threshold voltage.

When $V_d > V_g - V_{th}$ further increases in V_d will not effect the drain current, and the device enters what is called the saturation region. In the saturation region, the drain current is expressed as: $I_d = \frac{\mu_{eff} C_{ins}}{2} \frac{W}{L} (V_g - V_{th})^2$. Details about MOSFET and TFT I_d–V_g characterization are referenced in [10-12].

The threshold voltage can be obtained from I_d–V_g curves either in the linear region or in the saturation region.

From the linear region of I_d–V_g characteristics, V_{th} is obtained as the intercept and the field effect mobility; μ_{eff} is proportional to the slope of I_d–V_g in the above threshold region (where $V_g > V_{th}$). In a similar way, from the saturation region V_{th} and μ_{eff} are obtained from a plot of $\sqrt{I_d}$ versus V_g (fig. A.3). Work about extraction of subthreshold, threshold and mobility from I_d–V_g characteristic of TFTs is referenced in [13]. For fastness, the extraction of V_{th} and μ_{eff} from the linear region has often been used in this thesis; comparing these results with the results obtained from the saturation region a minimal 5 % error of accuracy is noticed.

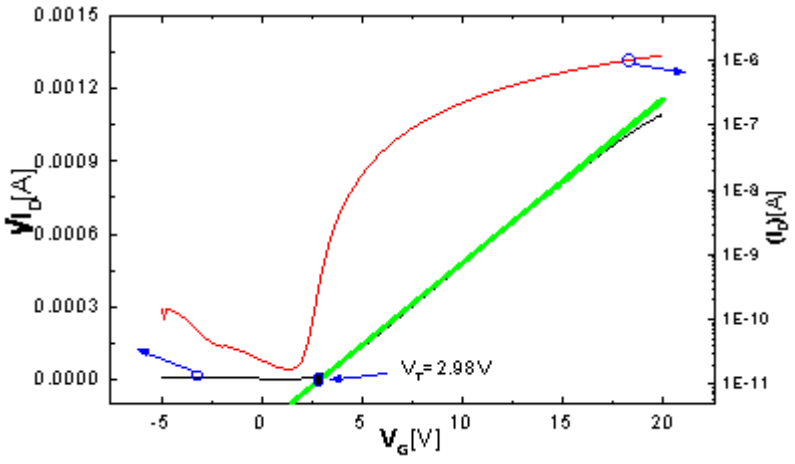

Fig. A.3. I_d–V_g characteristics of fabricated TFT 4 (L=40 μm, W=140 μm) in the saturation region. The drain voltage is 15 V.

The linear I_d–V_g characteristic has been used in this thesis (chapters 4, 5) as well to calculate the shift of threshold voltage after periods of gate voltage stress (fig. A.4).

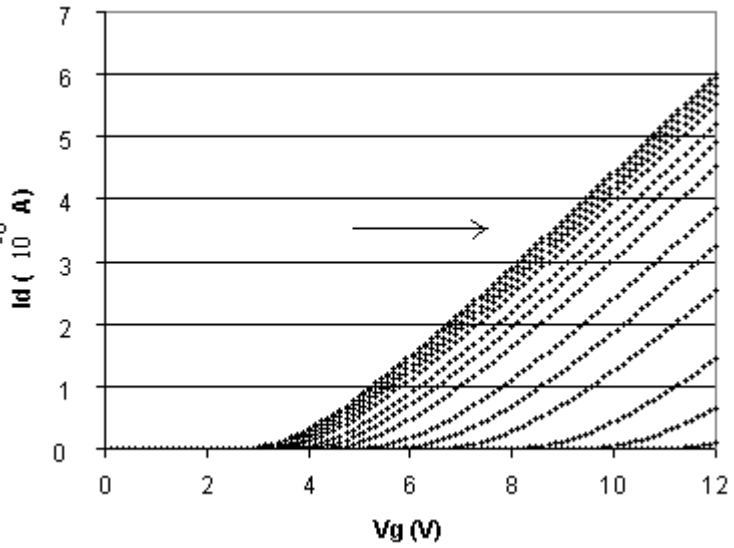

Fig. A.4. Transfer characteristics after a positive stress on the gate. The arrow indicates the direction of the shift. The device (W/L = 500/100) has been subjected to +35 V gate bias stress for a total time of 24 h.

The gate voltage stress has been applied by an external source and maintained during a pre-determined period. The characteristics have been measured again after voltage stress and the difference between initial V_{th} and V_{th} after the stress known as threshold voltage shift has been afterwards calculated by using MathLAB. The threshold voltage shift as function of stress time is presented in fig. A.5 for different TFTs used as device under test in this thesis.

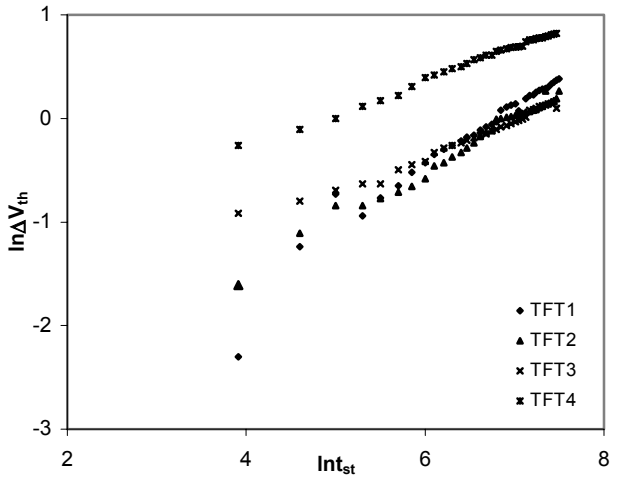

Fig. A.5. The dependence of the threshold voltage shift of four TFTs on the stress time.

The I–V measurements are used in chapter 3 to determine threshold voltage and mobility of a-Si:H/SiN TFTs. In chapter 4 and 5, I–V measurements under gate voltage stress are used to calculate the threshold voltage shift and respectively threshold voltage and subthreshold swing during stress. In chapter 6, a new technique, different from I–V characterisation has been used to measure I_{sd} current in-situ, during gate voltage stress.

Equipment used: 4156B Parameter Analyser for I_d–V_g curves in the saturation and linear regions and graphical programming language VeeTest for I_d–V_g curves after periods of stress. To measure I_{sd} during stress, 4156B Parameter Analyser has been controlled by ICCAP platform program (C++ programming language)

A.2.2. C–V measurements

The capacitance-gate voltage characteristic depends on whether the measurements are made at low (1 – 100 Hz) or high frequency (1 MHz). In this thesis, the device under test was a metal-insulator-amorphous silicon structure, MIAS (fig. A.6) deposited in the same wafer as TFTs i.e. the thickness of the SiN and a-Si:H films are almost equal like in the TFTs. MIAS is basically a metal-oxide-semiconductor, MOS structure where the insulator is other than SiO_2 (this case SiN) and the semiconductor is not crystalline but amorphous. Details about C–V characterization of MOS structures were found in the papers referenced in [10-12].

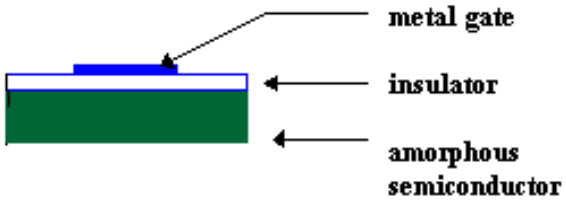

Fig. A.6. Cross section through a MIAS device

In the following, the names of accumulation, depletion and inversion regions of C–V characteristics are used to describe the behaviour of MIAS

even although they do not mean the same like in MOS. Some differences between C–V of MIAS and MOS capacitors are briefly presented below.

The quasistatic measurements have been performed at 10 Hz with a d.c. gate bias varied slowly from negative voltages towards positive voltages at dV/dt = 0.2 V. The high frequency measurements have been performed at 10^5 Hz with a superimposed a.c. signal.

In the MOS case when the semiconductor is crystalline, the interpretation of C–V measurements is quite straightforward since the accumulation; inversion and depletion regions are clearly described. In MIAS with amorphous semiconductor, the amorphous semiconductor is characterized by deep bulk states due to dangling bonds, which contribution to the total capacitance must be taken into account so that only the 'accumulation' has the same meaning like in MOS capacitor. The occupancy of deep states both interface and bulk a-Si:H states determines the space charge for any applied bias. DBs DOS is highly non-homogeneous and varies rapidly near a-Si:H/SiN interface due to band bending having a bump in the lower and upper part of a-Si:H gap respectively as explained in chapter 3, section3.3.

The quasistatic C–V curve looks different in MIAS capacitors comparing to the ones for MOS capacitors (fig. A.7) having just a shallow 'bump' in the depletion region instead of a clear minimum.

In this order of thinking, it is said that the 'bump' in quasistatic measurements of MIAS reflects the shape of bulk trap density.

The flat band voltage is not the 'true' flatband voltage that is difficult to be measured but an 'apparent' one as it was explained in chapter 5. From quasistatic C–V measurements, the flatband voltage has been obtained from the onset of depletion, like in MOS capacitor; the meaning of flatband being differently interpreted in this case as explained in chapter 5.

The high frequency curves of MIAS look like similar to the high frequency curves of MOS capacitors. In fig. A.7, for clarity, the high frequency curve was considered the same for MOS and MIAS but in reality, due to charge trapping, the curve stretches out along the y axis. The high frequency capacitance under accumulation conditions is the same as the insulator capacitance. The 'depletion' is reached when the large majority of charge is trapped by interface/bulk defects in the semiconductor. The interface and defect trapped charge have time constant too low to follow the signal therefore

the total capacitance decreases until a minimum given by the total (interface and bulk) defect density. Finally, as the gate voltage increases, these trapping sites are filled with carriers and do not trap anymore, 'inversion' occurs at the interface meaning that more carriers are attracted from the a-Si:H bulk than can be trapped in defects and the capacitance restores to the capacitance in accumulation.

The quasistatic curves performed in this thesis on MIAS capacitors look different from those of a MOS capacitor, presenting a shallow minimum of capacitance in the 'depletion' region. This minimum is associated either with negative or with positive charged defects as the defect equilibrated under electron or under hole accumulation [14].

Other authors reported even two clear minima that appear when experiments are performed under thermal bias annealing conditions [14]. With bias annealing (explained in chapter 5), the density and spatial distribution of bulk defects can be changed and the two minima of capacitance correspond to positive in the upper part of a-Si:H gap and negative charged defects in the lower part.

Coming back to room temperature measurement, like in the case presented in this thesis, the C–V shows only one minimum that is associated with negative charged defects as the defect equilibrated under electron accumulation. When the MIAS device is subjected to stress at room temperature this minimum shifts to more positive or negative voltages according to the sign of bias polarity i.e. towards negative voltages under negative voltage stress or towards positive voltages towards positive stress. In the case of negative stress the shift results in an increase in positive charge in the semiconductor due to created positively charged DBs and the reverse holds for positive stress.

However, the V_{fb} extracted from quasistatic C–V measurement of MIAS should be regarded as a qualitative measurement rather than a quantitative one, because the equipment used to measure the current and to calculate the flatband voltage was one dedicated to C–V measurements on MOS structures. Therefore some of the constants needed in the calculation were considered the same as in MOS capacitor E.g. the exact work function between the metal (Al) and the semiconductor (a-Si:H) was not known and it was considered equal to the work function between Al and Si.

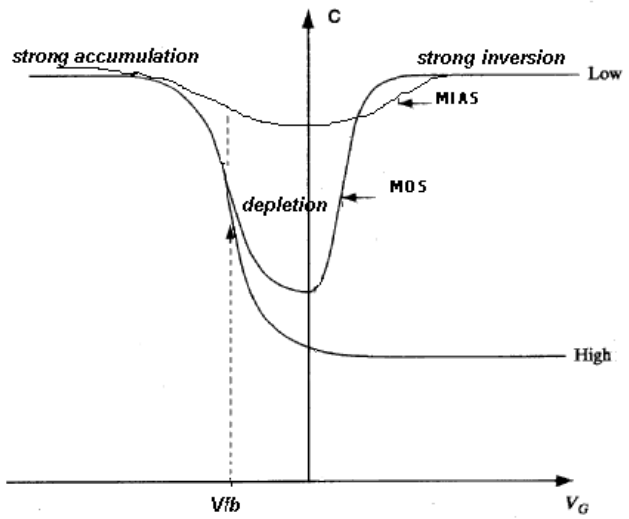

Fig. A.7. C–V measurements of a MOS and MIAS capacitors.

The C–V measurements are mostly used here to show the effect of a period of gate stress on the flatband voltage (namely the shift of the apparent flatband) in chapter 5. Quastistatic and high frequency measurements have been performed as well in chapter 7 in addition to deep level transient spectroscopy and slow trap profiling

Equipment used: HF: 4275A multifrequencymeter and QS: 4140B picoamperemeter. The flat band voltage was automatically extracted from the capacitance-voltage measurements (HP Parameter Analyser 4140B connected to Karl Suss Probe Station) by MDC CSM/Win System package. To study the effect of stress on the capacitance, an external source had been connected to the gate.

A.3. Traps characterisation

The activation energy and density of traps at the interface in a-Si: H and SiN have been determined using charge-Deep Level Transient Spectroscopy (QDLTS) and Slow Trap Profiling (STP). QDLTS is used for characterisation of the traps in a-Si: H and STP for traps in SiN. QDLTS and STP basics are described in chapter 7.

A.3.1. Charge Deep Level Transient Spectroscopy (QDLTS)

Deep gap ambipolar defects (positive, neutral and negative charged defects) are important in semiconductor devices since they can act as traps as shown in section A.2 and chapter 2. QDLTS has been used in this thesis (chapter 7) to characterise the a-Si:H traps. General theory of QDLTS is referenced in [15]. The devices under test are special MIAS capacitors with thickness of insulator and semiconductor 10 nm and 1 μm, respectively.

QDLTS is based on measurement of the transient response of the carriers emitted from bulk traps under periodically applied voltage steps to the gate electrode. The sample is heated at a constant rate and the current associated with thermal emission of trapped carriers flows in the external circuit until the trap occupancy is restored to its initial steady state. Therefore, the emitted charge as a function of time is recorded in spectra of temperatures. In these spectra, a peak corresponds to a trap level active at that temperature. The height of the peak is proportional to the trap density. The activation energy and cross section are obtained from an Arhenius plot of the emission times versus temperatures at which peaks appear [16, 17]. The results of QDLTS investigation on special MIAS are presented in chapter 7.

Equipment used: A charge sensitive amplifier is used for charge-to-voltage conversion. The temperature of the sample is varied using a liquid nitrogen cryostat.

A.3.2. Slow Trap Profiling (STP)

STP has been used to characterise SiN and interface traps. Traps in SiN are either in the insulator bulk or at the insulator/semiconductor interface. Traps at the interface are switching states that, during electrical stress, exchange charge with a-Si:H channel they are faster that insulator bulk traps but slower than traps located at the interface in a-Si:H. details bout these traps were found in reference [18].With STP it is possible to determine the density of the traps located at the interface insulator/semiconductor in the insulator and their energy position. Devices under test were MIAS capacitors on the same wafer as TFTs.

STP performs two functions: a quasistatic C–V measurement and the measurement of the charge transients. A staircase voltage signal is applied to the gate biasing from negative voltages towards positive voltages. A holding time and a flash of light is applied in order to ensure that the structure is in thermal equilibrium before the stepping starts. The quasistatic measurement is used to calculate the surface band bending and the energy position of the traps. Afterwards the gate current in time is measured at a variable delay time after each voltage step. The current is proportional to the charge emitted from the slow states in time. A charge profile function of time and applied gate voltage is obtained as a 3D graph. Integrating by time and voltage the charge profile, the slow trap density (cm^{-2}) is obtained also as a 3D graph. The results of STP measurements on MIAS capacitors subjected to periods of gate voltage stress are shown in chapter 7. A detailed work with STP for MOS capacitors is referenced in [19, 20].

Equipment used: The voltage stepping and current response measurements were obtained using an HP4145B parameter analyser. Step time was 50 ms, holding and delay time were 0 s. Voltage step was 0.2 V or 0.1 V. The hardware includes STP box, digital I/O interface and I/O card that plugs into IBM PC. The software is written in Visual Basic.

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SUMMARY AND CLOSING REMARKS

As it had been shown in the introduction of this thesis, nowadays a-Si:H TFTs function adequately for LCD as well as in many new microelectronic and opto-electronic applications. The current driving force in the research and development of TFT-LCDs is to integrate the driver circuitry onto the display board, to improve reliability and reduce costs. LCDs incorporating hydrogenated amorphous silicon a-Si:H TFT technology are currently produced on glass substrates were the deposition of a-Si:H requires a substrate temperature of about 200 °C. Plasma enhanced chemical vapor deposition, PECVD, is the only practical large area, low temperature, high throughput fabrication method for a-Si:H TFT arrays today. The a-Si:H and SiN film properties and especially a-Si:H/gate SiN interface chemical and physical properties are critical to the TFT characteristics.

This work addresses the fabrication and the study of a-Si:H/SiN TFTs instability at room temperature due to degradation induced by low gate voltage stress.

Inverted staggered TFTs with a-Si:H deposited at two different powers (60 and 100 W) and SiN deposited at the same powers as a-Si:H and in different nitrogen gas flow were fabricated. The deposition aimed to fully amorphous a-Si:H and stoichiometric or N-rich SiN. X-ray diffraction, Fourier Transform Infrared Spectroscopy and Rutherford Backscattering (XRD, FTIR, and RBS, respectively) thin film characterization techniques prove that the deposited a-Si:H is fully amorphous Si. However, in the samples deposited at 100 W the concentration of H in a-Si:H increases with respect to the sample deposited at 60 W and, as a consequence, the density of volume defects due Si dangling bond increases. The characterization shows a SiN_x with a stoichiometry (x) varying from 0.86 to 1.26 (that corresponds to below stoichiometric to near stoichiometric SiN) that has been deposited. It has been proven that, by increasing N_2 flow, SiN closer to stoichiometry (stoichiometric nitride Si_3N_4, has x = 1.33) and above stoichiometric, N-rich SiN, can be obtained by increasing the N_2 flow in the PECVD reaction chamber. The capacitance-voltage measurements of Al/Si/SiN/Mo structures show that when SiN is close stoichiometric, the threshold and flatband voltages are lower than in the structures made with below-stochiometric SiN, indicating an insulator with less charge trapping sites.

The TFTs made with these a-Si:H and SiN films are n-channel devices characterized by a mobility between 0.17 to 0.22 cm^2/Vs, a positive threshold voltage ranging from 3.5 to 5.5 V and a negative flat band voltage between −8 to −2 V. FTIR of the a-Si:H/SiN interface show an enhancement of high dihyrides peaks (SiH_2 and NH_2) in the TFTs made with below-stoichiometric SiN.

The transfer characteristic of TFT have been modeled after solving Poisson' equation for the case with DBs in a-Si:H gap and without. Other calculations resulting from modeling such as the volume density of free carriers and band bending function of applied gate voltage have been done. It has been theoretically demonstrated that the field effect mobility and the drain current decrease whereas the threshold voltage increases in presence of DBs.

The TFTs were subjected to various gate voltage stresses for a different period of stress time. For comparison of the experimental work, TFTs with N-rich SiN and non-inverted staggered commercial TFTs have been used.

The experimental threshold voltage shift obtained after stress as function of stress time has been fitted with two models from the literature. One of the two models ascribes the changes of the threshold voltage to charge trapping in SiN transitional region whereas the other one attributes the changes to creation of defects in a-Si:H. The fitting of these more or less simple experimental results is good for both models in the sense that both the charge trapping and defect creation are likely to occur. Therefore fitting of experimental data did not definitely conclude upon the mechanism that prevails in threshold voltage shift degradation.

In order to see which mechanism prevails in the degradation of threshold voltage shift at room temperature, the threshold voltage, the flat band voltage and the subthreshold slope had been measured using capacitance - gate voltage, C–V, and drain current - gate voltage, I–V, measurements. The changes of subthreshold voltage and flatband voltage during prolonged gate voltage stress were correlated with the corresponding changes of the threshold voltage. The results have shown that the magnitude of changes of the subthreshold voltage during positive gate voltage stress corresponds to the magnitude of the changes in the threshold voltage. During negative stress, the changes in the flatband voltage correspond to the changes in the threshold voltage. But for both polarities of the stress, the subthreshold and flatband changes contribute to the total threshold voltage shift. According to this result, the gate voltage stress at room temperature cause degradation at the interface rather than in the bulk of a-Si:H.

Because I–V characterization and extraction of the threshold voltage is a laborious procedure, instead of calculating the threshold voltage after each period of gate voltage stress, the drain current in the linear region of I–V characteristics is measured 'in-situ' during stress. When the mobility is constant, the drain current in the linear region is proportional to the threshold voltage. By directly measuring the drain current, the intermediate step of I–V characterization that is necessary for the extraction of the threshold voltage is eliminated. The method avoids voltage stress during characterization being particularly good for the TFTs with large threshold voltage (> 6 V) when I–V characterization should sweep to gate voltages larger than 10 V in order to measure accurately the threshold voltage. The measurement method is also used to determination of mobility and threshold voltage in a similar way as in an I–V characterization. It has been proven that the changes in the drain current are due to changes in the threshold voltage and not to changes in mobility.

All parameters of the current measurement (time intervals an voltages) are software-controlled (ICCAP platform program) and can be set at the beginning of the measurement. The measurement method is flexible allowing alternative periods of stress and relaxation at pre-selected time intervals. It has been shown that the two previously mentioned models do not fit the complex results obtained after sequences of positive, neutral and negative stress.

A new model that combines defect creation at the interface in a-Si:H and charge exchange between a-Si:H channel and SiN transitional region at the interface was proposed to explain the experimental data. It has been demonstrated that only with two parameters: the volume density of charged defects and the dispersion coefficient, the model explains the degradation and recovery of the drain current during positive and negative gate voltage stress.

The degradation of the drain current and threshold voltage is more evident in Si-rich SiN than in the N-rich SiN due to more trapping sites present in sub-stoichiometric SiN. Apparently, less current degradation is achieved by subjecting the TFTs first to a period of negative stress due to detrapping of negative charge trapped from SiN border traps.

In order to find out the nature, the energy position and the time response of the traps that are involved in the room temperature electrical induced degradation, QDLS and STP measurements have been carried out. The results of these measurements have shown that the a-Si:H dominant interface defect is the neutral defect that lies around a-Si:H midgap and that is active above 400 K and that the charge exchange between a-Si:H channel and SiN transitional region is

mediated by border traps that are traps with time constants lower than the interface traps. The results show as well that by subjecting the TFT to a long period of stress time (>12 h) even at low gate voltage stress (10 V) the charged border defects or slow traps increase their density due to exchange with the a-Si:H channel.

The experimental techniques and the equipment used throughout the thesis to characterize the a-Si:H and SiN films (FTIR, RBS and XRD), the TFTs (I–V and C–V characterization) and the traps involved in TFTs' degradation (QDLTS and STP) are explained and mentioned in the Annexe.

Based on the results summarized above and detailed in the 'conclusion' section at the end of each chapter, the electrical induced degradation at room temperature and low stressing voltages is an interface related phenomena, a combination between defect creation and charge trapping/detrapping of the carriers from the channel to the border traps in SiN.

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ANDREEA